

# videoDSP

## 388VDO Video DSP

Fully programmable, ideal for mobile handset and personal media players

PRODUCT BRIEF

### FEATURES

- Video codec processor for consumer entertainment devices
- Fully software programmable in C/C++
- Rich software tool chain
- Supported by a library of most common codecs
- Capable of encode and decode in real time
- Optimized for block-based codecs
- Very low power, low area
- Simulation model with video test streams available for evaluation and software development
- FPGA prototype available for demonstration and evaluation

### BENEFITS

- One DSP for all codecs
- Programmable for new or changing standards
- Low power and small area footprint is ideal for portable and mobile applications
- Pre-packaged, ready to drop-in module for easy integration into SOC designs
- Custom video specific instructions for better code density and fewer cycles

### Market Overview

Digital video first hit the consumer market in 1997 with the introduction of DVDs based on the MPEG-2 standard. In the short span of 10 years, digital video has made both VCRs and analog camcorders obsolete. Digital video is now pervasive in everyday life, from DVDs of Hollywood movies to user-created content on the Internet. This has been enabled by the tremendous pace of semiconductor technology continually driving costs down and capabilities up.

The advance in semiconductor complexity has, at the same time, enabled the development and deployment of newer and better video codecs that offer both higher quality and higher compression rates (H.264, MPEG-4, VC-1/WMV9). Technology has now reached the point where DVD quality products can be developed for mobile applications such as cell phones and portable media players.

### High Quality Video — Ideal for Mobile Handsets and Personal Media Players

Tensilica's 388VDO Video DSP is fully programmable to support all popular video codecs up to D1 rates including H.264 Main and Baseline profiles, VC-1 Main and Simple profiles, MPEG-4 Advanced Simple profile (ASP) and Simple profile (SP), and MPEG-2 Main profile, each of which is available from Tensilica's industry leading codec library. Lower resolutions such as QCIF, QVGA, CIF and VGA are also supported. This makes the 388VDO Video DSP ideal for mobile handsets and personal media players.

## 388VDO Video DSP

The 388VDO Video DSP performs all of the key video processing functions in software on the cores – including the network abstraction layer, picture layer, slice layer, bit-stream parsing and entropy decoding and encoding. This includes the computationally demanding CABAC (Context Adaptive Binary Arithmetic Coding) decoding in the H.264 Main profile decoder that other video engines omit, implement in a complex non-programmable hardware block, or implement in a general-purpose CPU that must run at over 700 MHz, significantly increasing power consumption. By implementing CABAC in the processor's instruction set, Tensilica offers a low MHz and power-efficient version of CABAC in less than half the area of a typical CABAC hardware block.

The 388VDO DSP offers both Baseline and Main profile solutions – Main profile offers superior data compression and video quality and is the preferred coding scheme at resolutions of D1 and higher for advanced handset and PMP applications.

## Full Software Suite Including Encoders and Decoders

Tensilica has developed encoders and decoders for the 388VDO DSP, so these are complete solutions with the hardware and software available directly from Tensilica. SOC designers do not need to rely on third-party application providers. The following are available from Tensilica for the 388VDO:

- H.264 Baseline profile decode
- H.264 Main profile decode
- JPEG Baseline decode
- JPEG Lossless decode
- MPEG-2 Main profile decode
- MPEG-4 Simple profile decode
- MPEG-4 Advanced Simple profile decode
- Real Video 9, 10 decode
- VC-1/WMV9 Simple profile decode
- VC-1/WMV9 Main profile decode
- H.264 Baseline profile encode
- JPEG encode
- MPEG-4 Simple profile encode
- MPEG-4 Advanced Simple profile encode

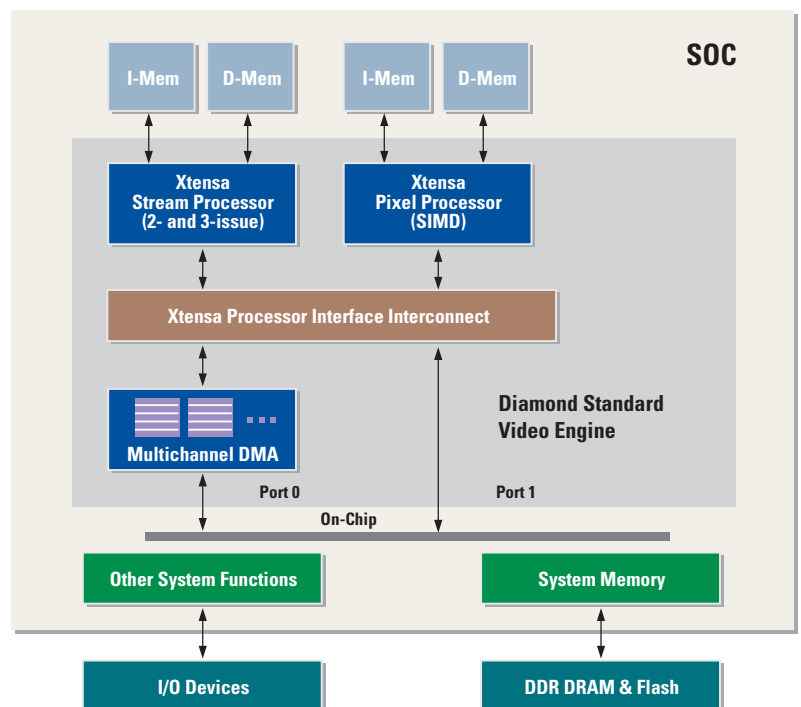
Tensilica also provides a complete matching software development tool chain including an advanced integrated development environment based on the Eclipse framework, a world-class compiler, a cycle-accurate SystemC-compatible instruction set simulator, and the full industry-standard GNU toolchain. In addition, Tensilica's wide partner network provides operating systems, debug probes, ICE solutions, and other support needed to program Tensilica's processors quickly and easily.

The following diagram illustrates the implementation of the 388VDO Video DSP. The 388VDO consists of two heterogeneous processors, a stream processor and a pixel processor, which are both Xtensa processors enhanced by application-specific instructions, a point-to-point interconnect, and a multichannel DMA controller.

The stream processor is accelerated for serial processing such as bitstream parsing, entropy decoding, and control functions. The pixel processor works on the data plane and performs parallel computations on pixel data using a single instruction multiple data (SIMD) instruction architecture. Both processors have different local memory and data width configurations as required by their functional partition.

The processors also can read and write from each other's local data RAMs, but most of the data movement between the processors and memories is performed by the DMA engine. It can be set up to do chaining DMA with circular descriptor buffers. It has 5 channels, each one can queue up multiple DMA operations and has an intelligent arbitration scheme based on programmable bandwidth allocation per channel.

## Block Diagram



The Processor Interface (PIF) interconnect block is a high bandwidth, low latency crossbar capable of transferring data at 3.2GB/sec., connecting all the video decoder components and the system ports together. The 388VDO connects to the system memory controller through two ports with identical processor interface (PIF) protocols and communicates with the system controller through shared memory API.

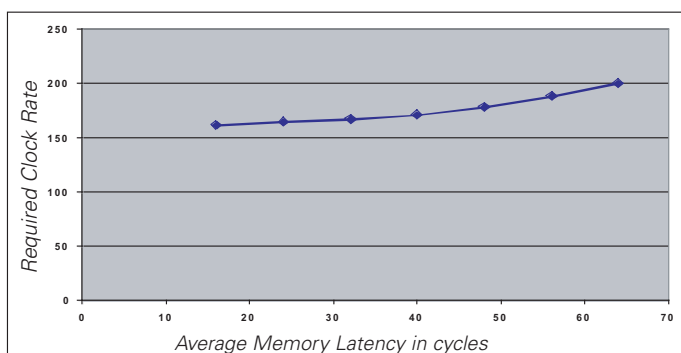
The 388VDO can be configured with an optional bridge to AMBA standard SOC interconnects.

## The Flexibility of Processor-Based Video Decoding

The 388VDO includes over 400 video-specific instructions to significantly boost performance compared to general-purpose DSPs or general purpose 32-bit microprocessors. These instructions are optimized for the most performance-intensive algorithms used in video processing, including:

- CABAC, which achieves higher compression in H.264 Main profile video
- CAVLC (Context-adaptive variable-length coding) used in the H.264 Baseline and Main profiles
- Deblocking, which reduces artifacts that appear in highly compressed video streams
- Transforms for spatial frequency compression
- Motion compensation and motion estimation, algorithms used to achieve high image quality at lower bit rates through prediction.

The 388VDO Video DSP compares favorably to the traditional approach of using pure hardware based video accelerators in tandem with conventional CPUs. The 388VDO offloads the full video decode task – including all elementary video bit-stream parsing – from the system host CPU. Conventional hardware accelerators only offload the pixel processing functions like motion estimation, and leave a large compute burden (often more than 100 MHz of continuous host CPU overhead) on the system controller.



By processing the entire video bitstream in a single module, the 388VDO Video DSP avoids wasting power in the system bus by shuffling data to and from a host CPU – power that is often not counted in power estimates of HW accelerator blocks.

When the 388VDO DSP is not being used to perform video tasks, it is a ready resource of over 500 Dhrystone MIPS of general-purpose CPU power available to perform other tasks – whereas dedicated video HW blocks cannot be reused.

The 388VDO DSP is programmable and, therefore, can host future and changing video standards.

The 388VDO DSP delivers all of these benefits in a compact footprint, consuming 6.6 mm<sup>2</sup> (including processor logic and local memories) in 90nm silicon processes.

## Low Area, Low Power Solutions for SOC Design

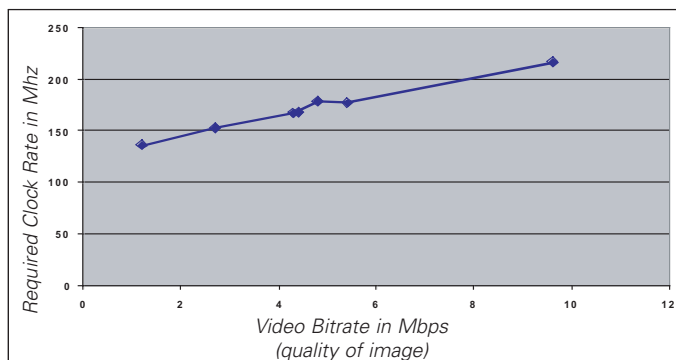
The 388VDO Video DSP is optimized for mobile applications and requires a smaller area and consumes less power than other cores.

Active power is further minimized through the use of fine grained clock gating, a feature of the Xtensa processor architecture, and the integration of power management instructions which provide programmability to throttle power under varying video work loads.

Additional power efficiency is achieved through the implementation of the DMA engine and interface to the Stream and Pixel Processors that minimizes the external memory bandwidth requirements.

The full-featured 388VDO delivers Main profile H.264 support for decode and MPEG-4 ASP encode at D1 resolution yet consumes only 6.6 mm<sup>2</sup>, including memories, in TSMC 90nm process technology.

The 388VDO, while decoding the “Foreman” H.264 Main Profile video stream, consumes 24.5 mW plus 9.7 mW for the memory, for a total power consumption of only 34.2 mW, based on TSMC 0.90G pre-layout with wireload estimates.



These charts are for decoding the “mobile calendar” sequence coded with H.264 Main Profile with CABAC at D1 resolution. The 388VDO is the most robust video processor core for difficult operating conditions and highbitrates.

## Video Performance Summary

Video Standard	Pixel Rate	Bitrate	Maximum Clock Rate Required*	DRAM Bandwidth	Power
H.264 Main Profile Decode	D1	5 Mbps	162 MHz	86.3 MB/s	59 mW
MPEG-4 Advanced Simple Profile Decode	D1	6 Mbps	167 MHz	59.8 MB/s	35 mW
VC-1/WMV9 Main Profile Decode	D1	6 Mbps	172 MHz	88.9 MB/s	50 mW
MPEG-2 Main Profile Decode	D1	8 Mbps	151 MHz	46.1 MB/s	38 mW
MPEG-4 Advanced Simple Profile Encode	D1	4 Mbps	188 MHz	148 MB/s	
Real Video 9 and 10	D1	2 Mbps	175 MHz		

\* Based on the "mobile calendar" video sequence in a TSMC 90G chip layout.

## Imaging Performance Summary

Imaging Standard	Pixel Rate	Maximum Clock Rate Required**
JPEG Baseline Decode	12 Mbps	200 MHz
JPEG Lossless Decode	10.5 Mbps	200 MHz
JPEG Baseline Encode	12 Mbps	200 MHz
JPEG Lossless Encode	10.5 Mbps	200 MHz

\*\* 8bits/pixel, YCbCr 4:2:0



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