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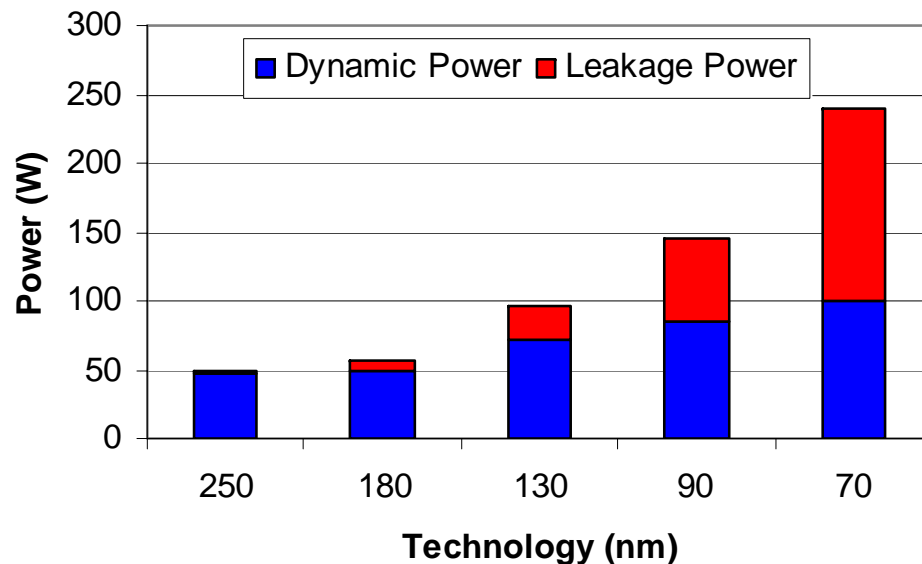
Implementing Power Management IP for Dynamic and Static Power Reduction in Configurable Microprocessors using the Galaxy Design Platform at 130nm

Dan Hillman, Virtual Silicon

John Wei, Tensilica

- Lowering dynamic power is not enough today
 - Clock gating helps, but it is only part of the total power solution
- In 130 and 90nm technologies, static power is approaching dynamic power
 - This presentation will show how to reduce dynamic power and static power as well

The Problem ...



Source: microprocessor power, Intel

The Challenge ...

- Reduce dynamic power and static leakage
- and maintain performance and cost goals

Current Solutions ...

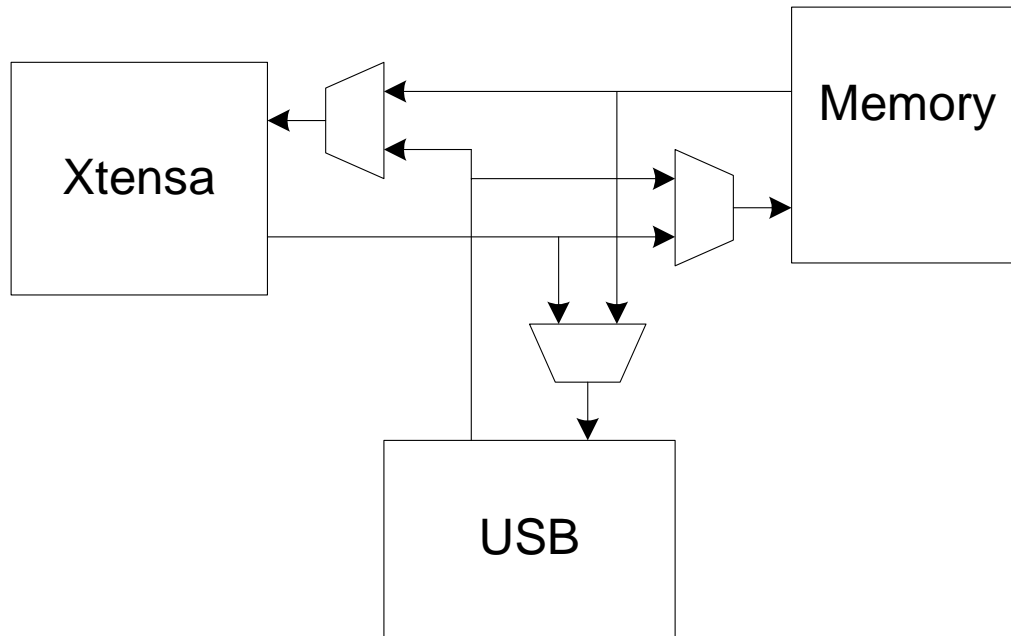
- Ad hoc, custom
- Not re-usable
- Results less than ideal



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Dynamic Power Reduction



- Divide SOC into functional blocks
- Run each block at a voltage low as possible



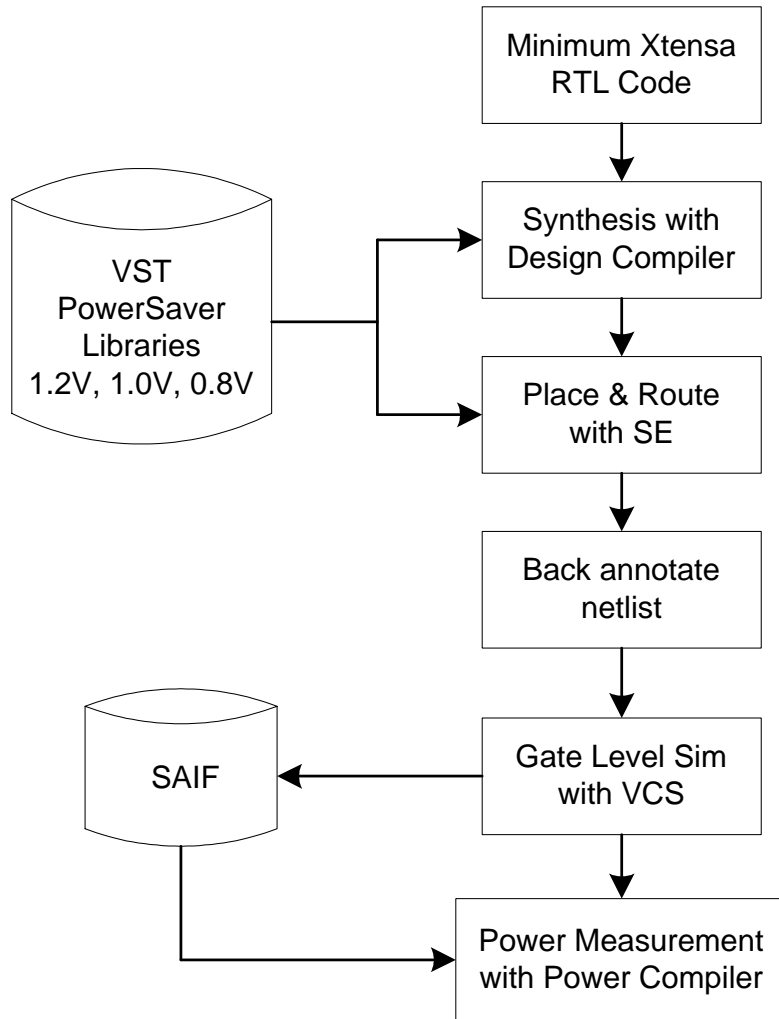
Minimizing Dynamic Power in the Xtensa Core

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- The system's performance requirements dictate the minimum frequency required by the processor.
- To minimize dynamic power, we are going to keep the frequency constant and lower the voltage as far as possible.
- Minimum Xtensa speed goal is 150MHz (6.67ns) WC post layout



- All designs were synthesized with wc wireload corner db
- Best case corner was used for hold time fixing.
- Routing done with 5 layers in a 6 layer system
- AC power numbers simulated with Power Compiler
 - No optimization was done with Power Compiler

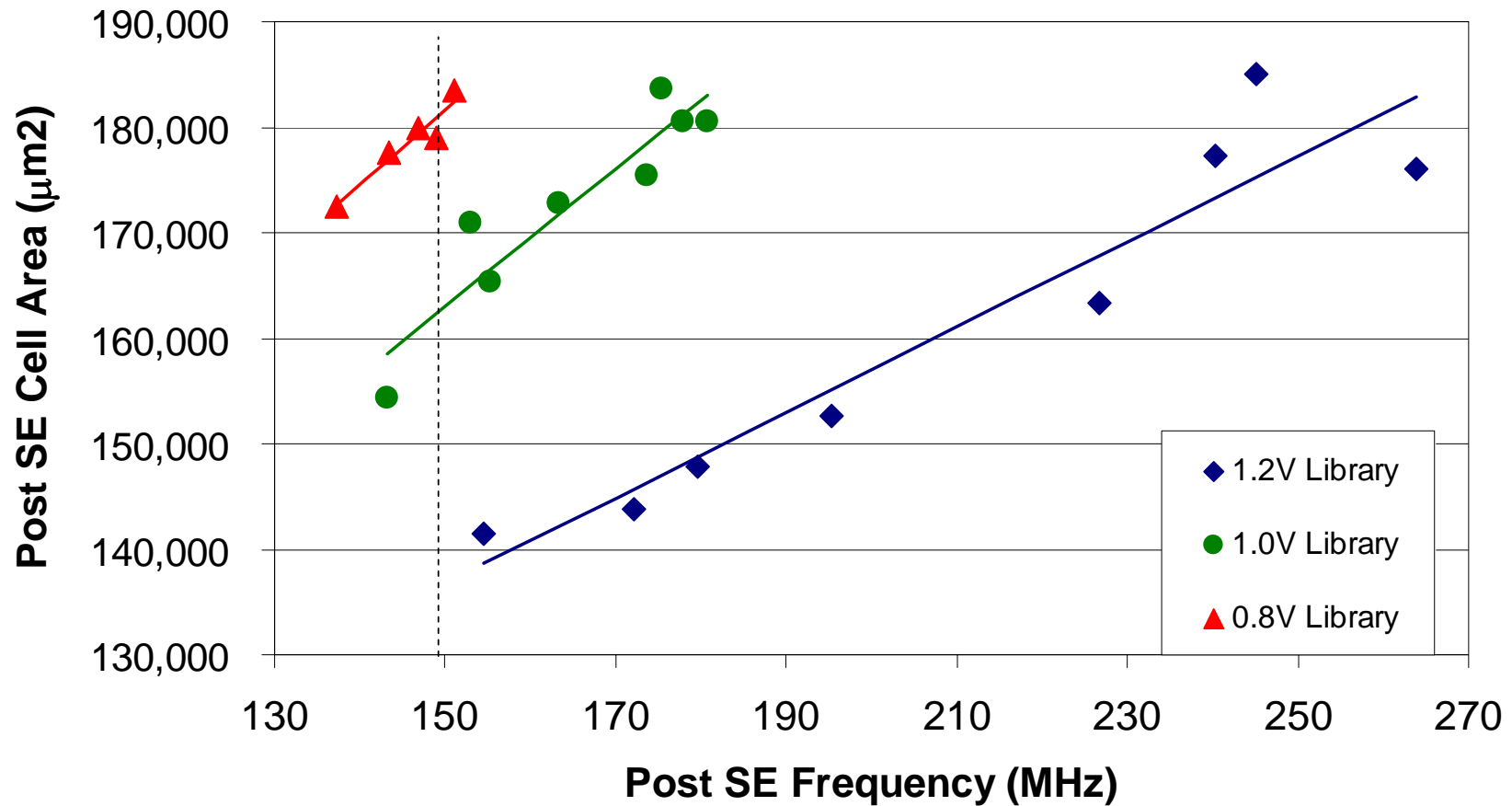


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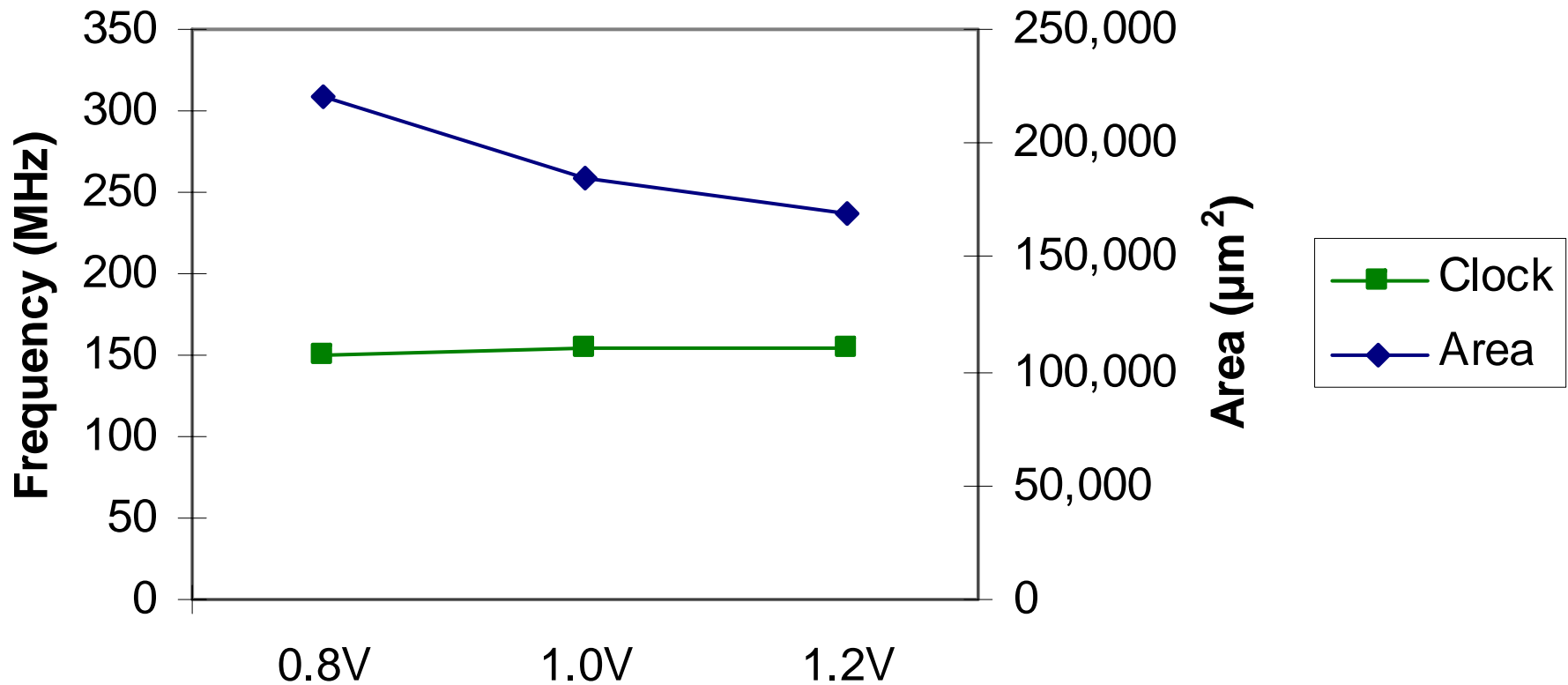
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Synthesis and Layout Results

Post Layout Frequency vs. Area

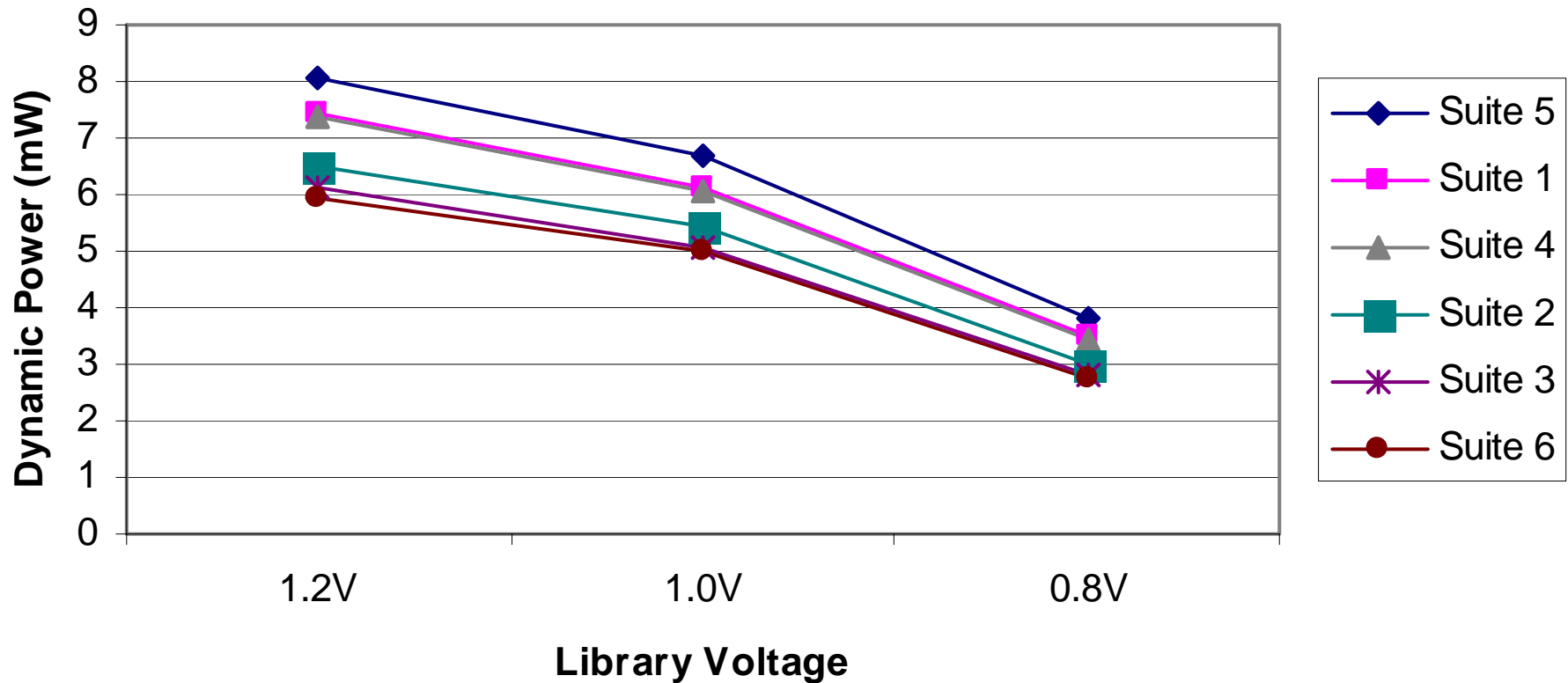


Post Route Results vs. Library

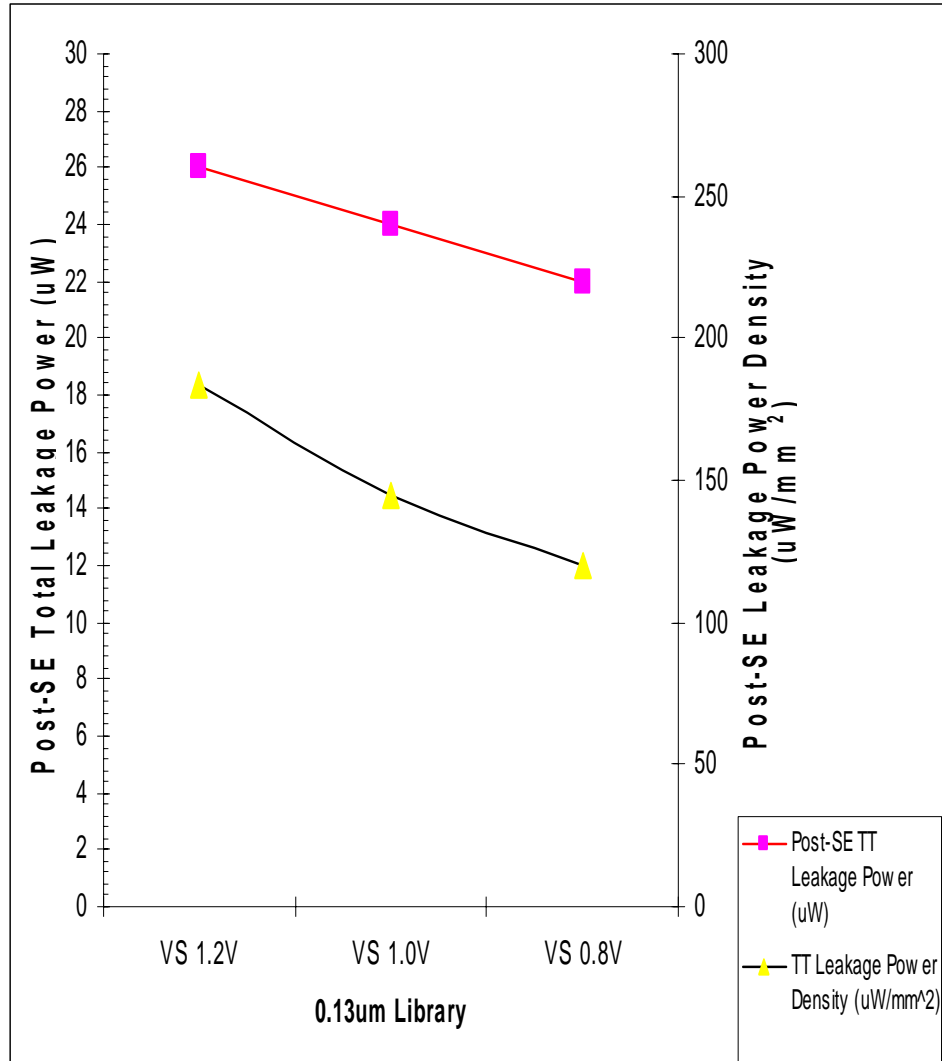


Dynamic Power vs. Voltage

- Compared to 1.2V
 - 1.0V achieves 17% power reduction with a 10% increase in area
 - 0.8V achieves 53% power reduction with a 31% increase in area



Scaled VDD – VDD Scaled Leakage Power Density



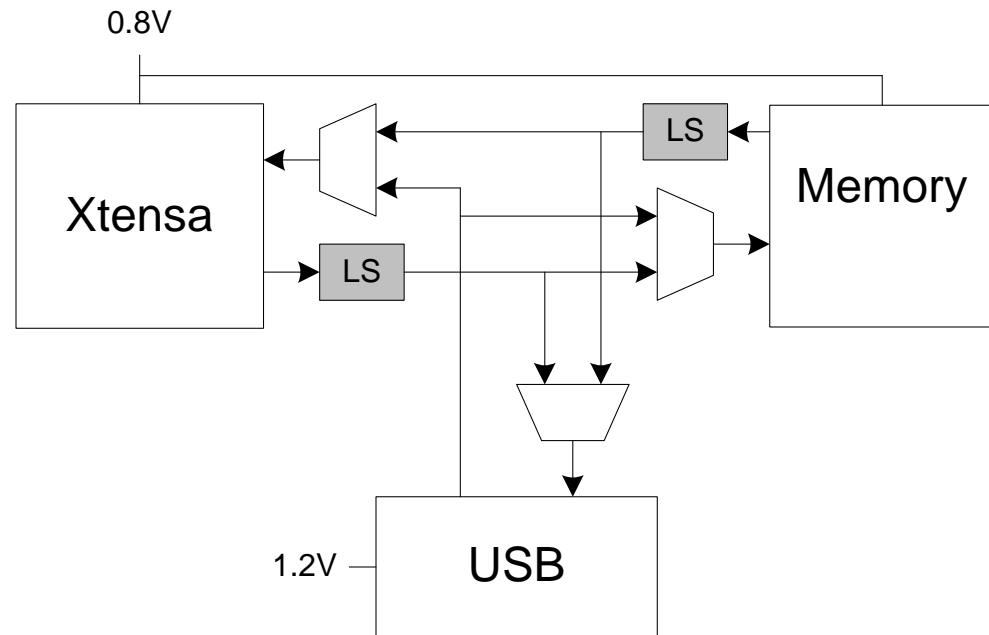
To achieve the same
150MHz post layout speed:

- Leakage power reduces with scaled V_{DD}
- Leakage power density (per unit cell area) scales with V_{DD}
 - The majority of leakage current is from sub-threshold diffusion current

Using Low Power Xtensa in an SoC

-
- We have reduced the dynamic power for the processor by lowering the voltage to 0.8V
 - How do I interface the 0.8V Xtensa and memory design with the rest of my chip?
 - Level Shifters

- Level shift the outputs of Xtensa and the Memory to 1.2V
 - Unique signals from the Memory to Xtensa do not need level shifting
 - Unique signals from the USB to Xtensa or Memory do not need level shifting
- Overdriving inputs of gates will cause no harm



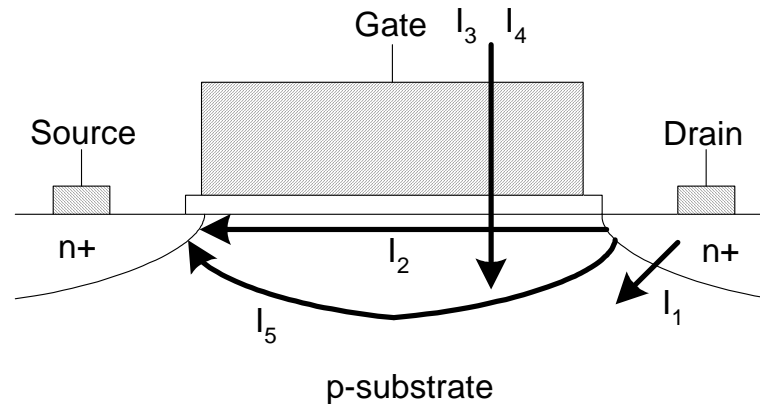
- The Xtensa core is able to achieve 150MHz post SE at 0.8V
- Compared to the 1.2V design, 0.8V design gives a 53% power reduction



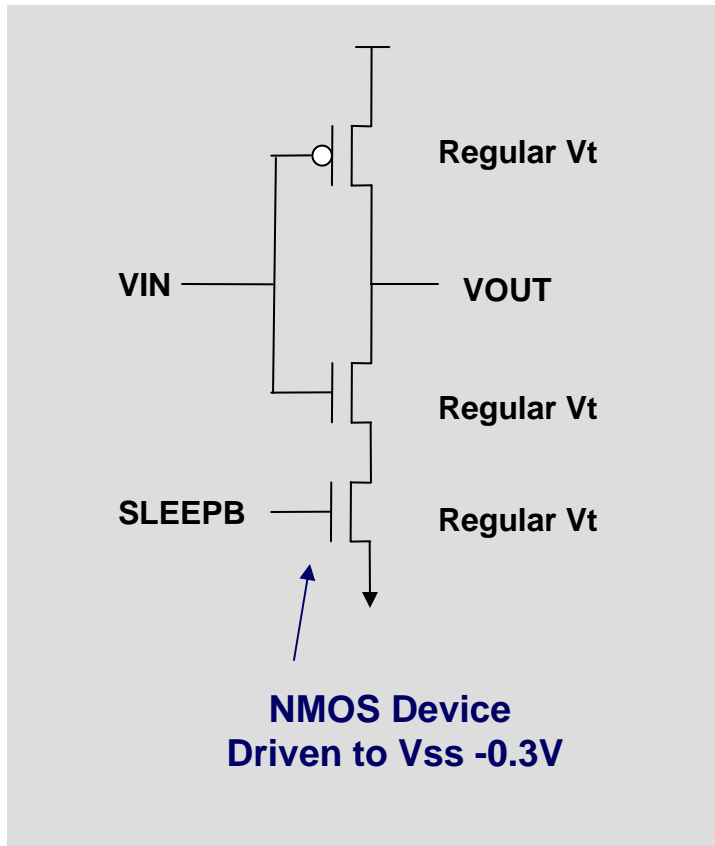
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Leakage Power Reduction



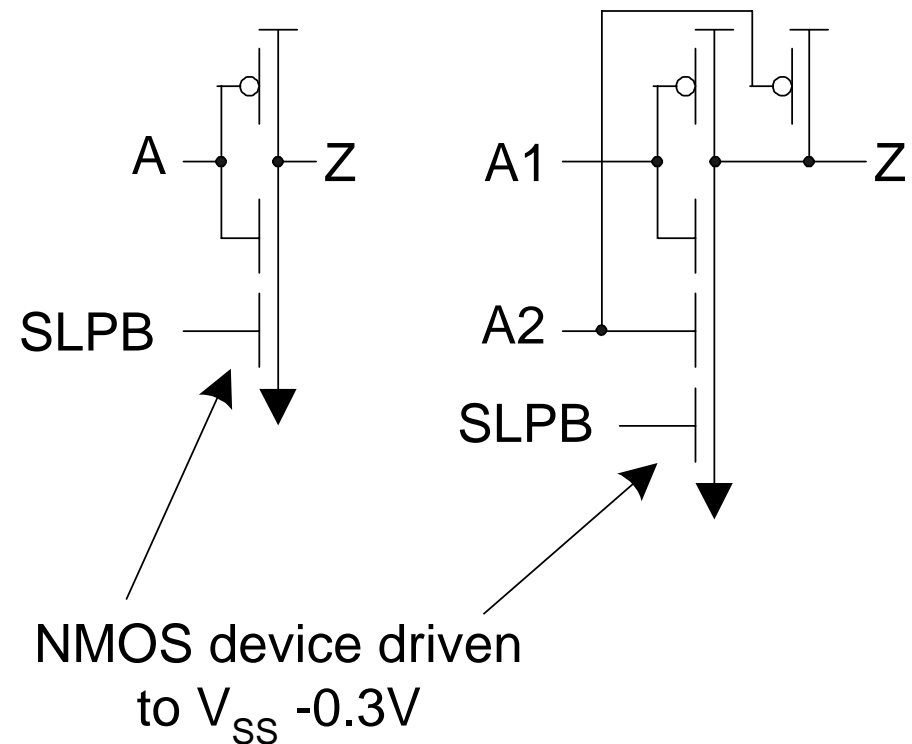
	<u>180nm</u>	<u>130nm</u>	<u>90nm</u>
• I_1 = reverse bias junction	minor	minor	minor
• I_2 = sub-threshold	minor	major	major+
• I_3 = oxide tunneling	minor	relevant	significant
• I_4 = hot-carrier injection	minor	minor	minor
• I_5 = off state leakage	minor	minor	minor



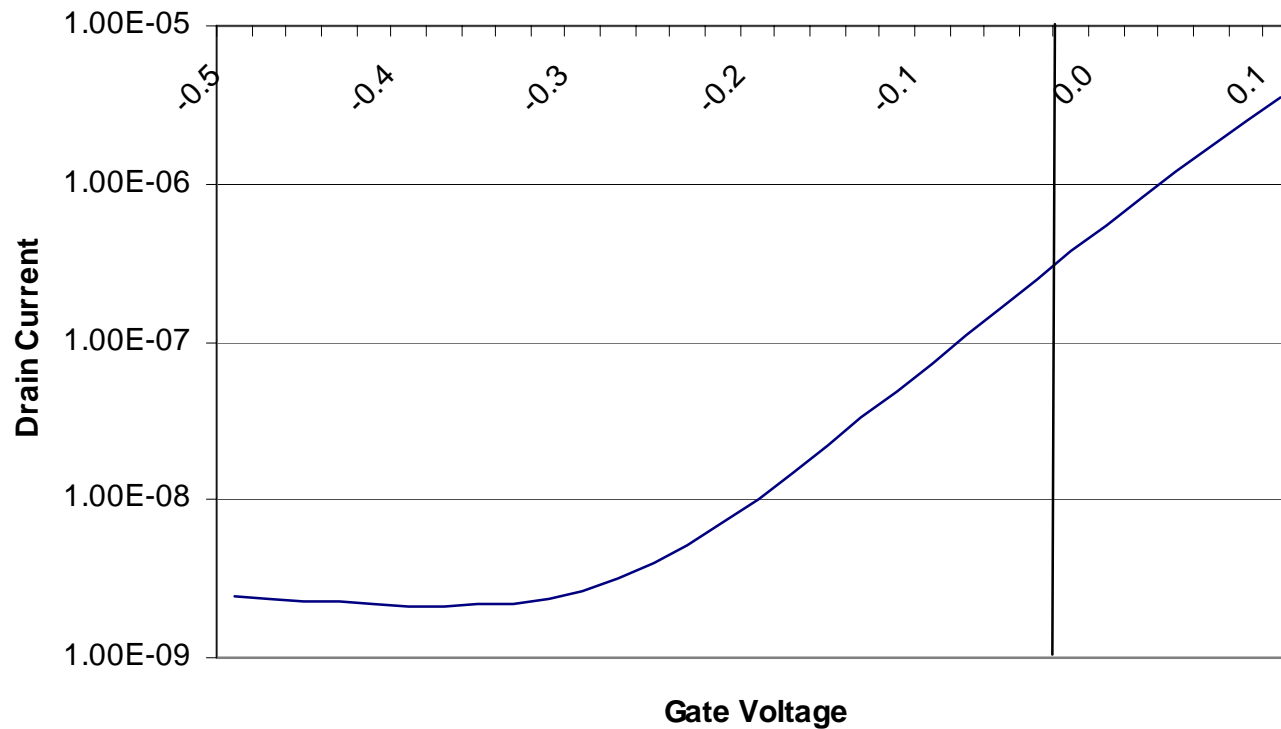
What is it?

- Add an NMOS *sleep device* in every cell
- Drive the gate of the sleep device negative
 - Decreases leakage current by ~250x
- Sleep can be used independently on modules
- Fast sleep and restore response time
- Data Retention Flip-Flops included
- On-chip generator creates and regulates sleep voltage.

- Sleep devices added
 - Inverter
 - NAND gate
- Sleep device shared for multiple paths in cells with multiple devices
- Larger cells have room for larger sleep devices
 - Speed impact small



90nm FF 125C



- At 0V gate bias, current is about 0.5μA
- At -0.3V gate bias, current is about 2nA
 - 260x reduction

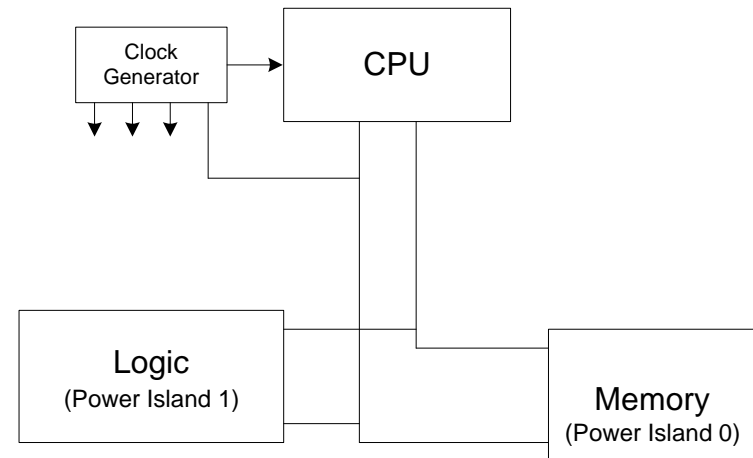


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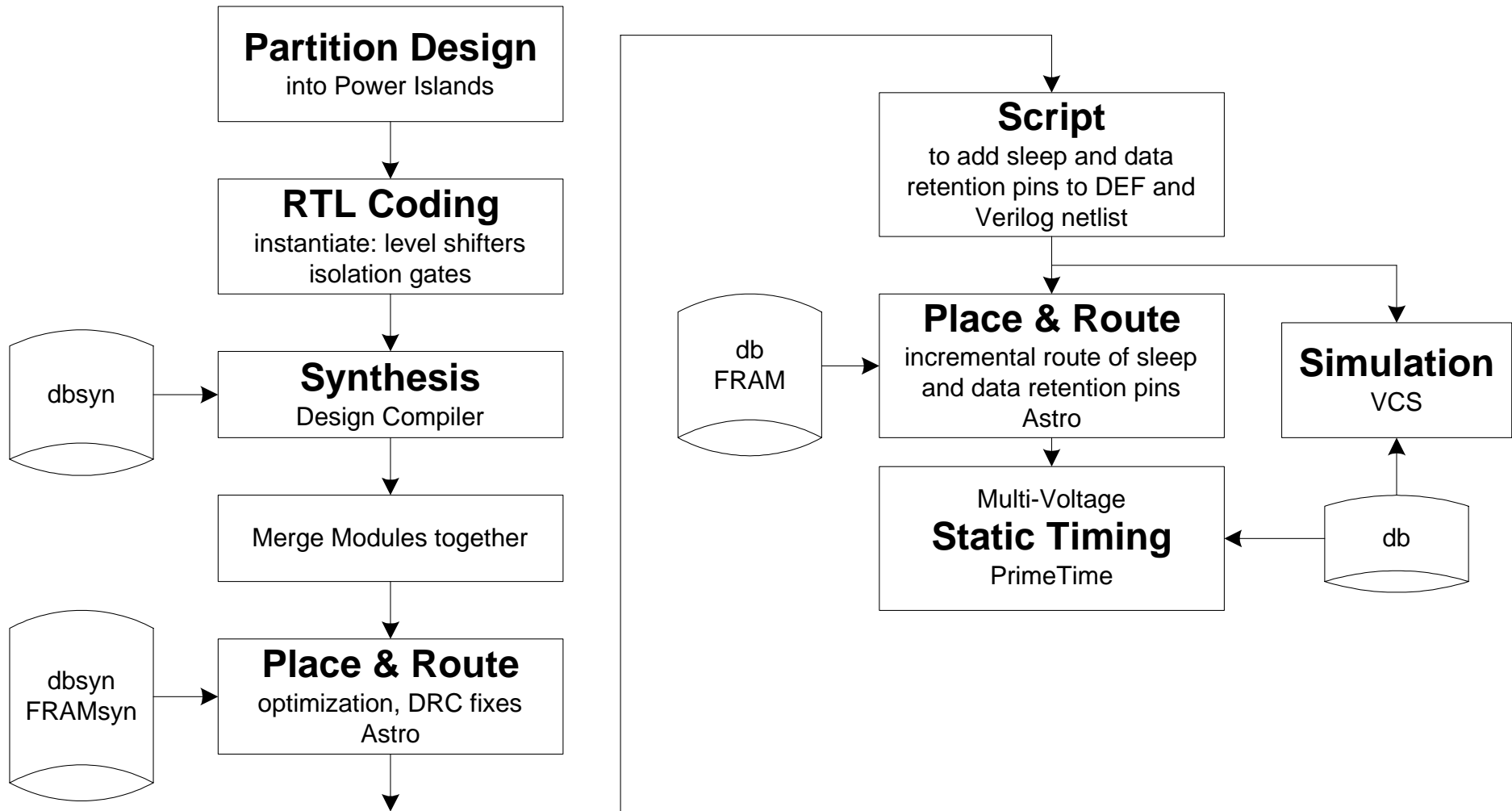
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Design Flow

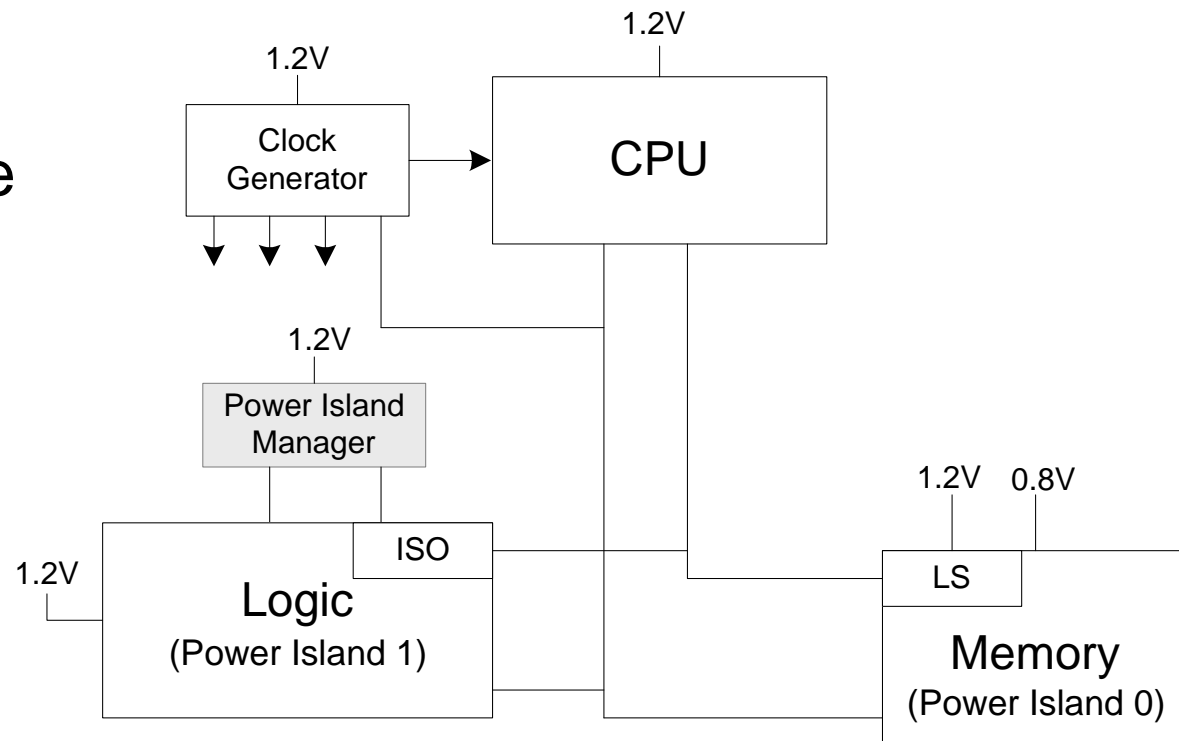
- Three modules
 - CPU
 - Logic
 - Memory
- Memory will meet performance requirements at 0.8V
- CPU is a hard macro and runs at 1.2V
- Logic module
 - Minimum frequency requirement is 200MHz



-
- Synthesis (DC) does not recognize sleep functionality
 - All sleep and data retention functionality is removed for synthesis
 - Current Design Flow requires two libraries
 - One without the sleep and data retention pins
 - One with sleep and data retention pins
 - Timing is the same for both libraries
 - Synthesize each power island separately
 - Script to add sleep and data retention pins to cells
 - Connect to Power Island Manager
 - Merge power islands

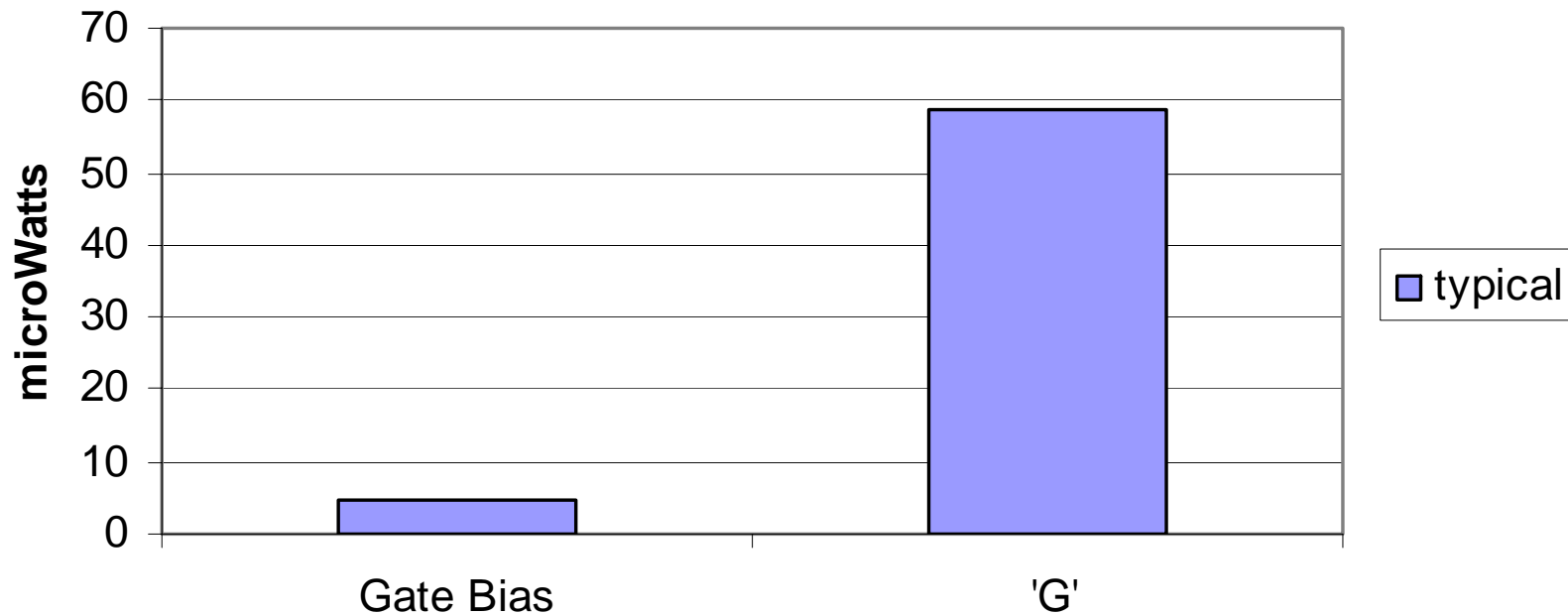


- Logic module would only run 200MHz at 1.2V
- Need to manage each island for
 - Isolation
 - Sleep
 - Reset of module
 - Data Retention



- Logic device contains approximately 108k devices and one Power Island Manager
- Power measured using 'Spice'

Static Power Comparison



Conclusion

- Dynamic power has been reduced by **53%**
- Gate Bias technology reduced peak static power by **92%**