

Chip summit highlights the way ahead

Escalating costs and the risk involved in having re-spins means there has been a huge decline in design starts for ASSP/Asics. So how will industry react? David Manners spoke to the men who know



Xilinx' Gavrielov: ASSP/Asic decline.



Mentor's Sawicki: Huge design costs.

The recent Globalpress Summit Conference in San Francisco highlighted many of the problems currently affecting the semiconductor industry.

"There's been a 40 per cent decline in the last four years in design starts for ASSP/Asic," says Moshe Gavrielov, CEO of Xilinx.

The rate of decline is so fast that, according to the CEO of eASIC, Ronnie Vashista, on present trends, there will be only 250 Asic design starts in 2030. The reason is escalating cost and risk - the \$50m cost of a chip, and the high chance of a re-spin.

Vashista's answer is to develop an architecture which permits the low-cost customization of an Asic using e-beam.

"We have developed a proprie-

tary architecture where a single via can be used to customise an Asic chip by direct-write e-beam," says Vashista, who believes his approach could "bring unique silicon back to the masses."

Could this stop the decline in Asic/ASSP design starts? Vashista thinks so. "I believe we are at an inflexion point where we're seeing a resurgence of Asic back into the mainstream," he says.

Not many agree. "Direct write gets you away from mask costs but those are dwarfed by the design costs," says Joe Sawicki general manager at Mentor Graphics

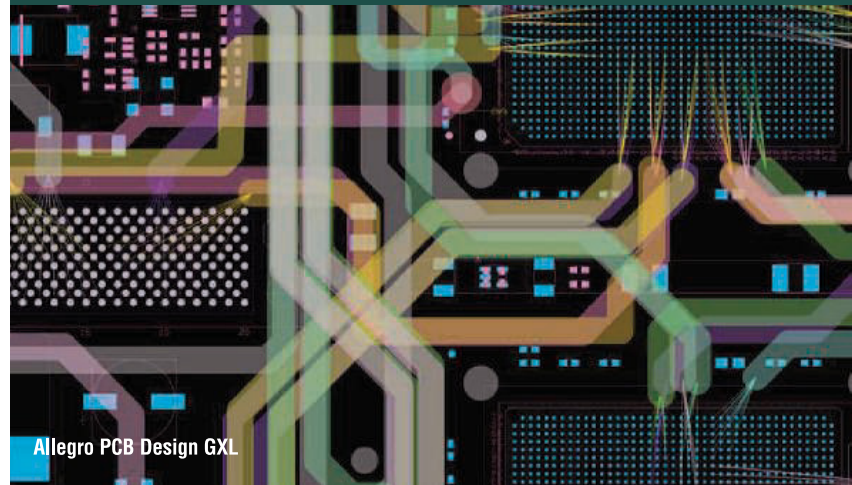
"A resurgence in Asic will require really significant cost reduction," says Andy Haines, v-p of marketing at Synplicity.

"Direct write will not be mainstream. It will not bring a resurgence

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eASIC's Vashista: Direct write e-beam.

→ in Asic. On the manufacturing side it has always been an available technology," says Walter Ng, v-p design enablement alliances at Chartered Semiconductor.

Another problem for Asics is difficulty of manufacture. "More than 50 per cent of Asics require at least one re-spin," says Gary Myers, CEO of Synplicity, "why don't the chips work? Most of the time it's a functional failure. The chip has not been verified properly. The failure can be reduced significantly with prototyping."

That maybe but, for the moment, the effect of the general disenchantment with Asic/ASSP is that venture capitalists are less keen to back chip start-ups.

"There's a tremendous decline in the number of semiconductor start-ups," says Myers, "not many make it to initial public offering (IPO). The exit strategies for investors aren't as attractive anymore. The up-front costs of \$40-\$50m are hard to substantiate."

And that's by no means all of the chip industry's problems. EDA tools are about to break down, according to Wally Rhines, CEO of leading EDA tools supplier Mentor Graphics.

"Adoption of new tools happens not when tools and flow don't work well, but when they don't work at all," adds Rhines, "that's when a company is forced to decide: 'What do I need to do to get the next design out?'"

The big question is, according to Rhines: "What is the next thing to break down?"

Rhines answers himself: "There's one out and out winner, place and



Mentor's Rhines: Place and route option.

route. It breaks down nearly every two generations. The existing tools cease to work. There's no question that place and route is the one that breaks next. Anyone doing 45nm is already struggling."

Agreeing, Jack Harding, CEO of eSilicon, says: "65nm is hard; 45nm is nearly impossible."

But Harding goes further than Rhines in declaring the EDA industry has problems and, as an former CEO of Cadence he knows about EDA. According to Harding, the EDA industry's business model is broken.

"In the EDA industry they sell the tools to the customer and, if the chip doesn't work, the EDA companies still get paid," says Harding, "the EDA industry is not sharing the risk of development. There's a fundamental disconnect in their business model, which is why they're having difficulty as an industry right now."

The EDA industry's business model contrasts with eSilicon's business model where eSilicon develops a chip at cost, then sells it for a margin on the silicon. "We make money by shipping silicon", says Harding, "we share the economic risks of our customers."

So, if an eSilicon chip doesn't work, eSilicon makes no money on its development. The same goes if the chip doesn't sell. That means eSilicon has to make a judgment call on its customers, and its customers' chip proposals, to ensure that they have a good chance of finding a market.

Another major problem could be emerging in the computer industry. Could another of Intel's business



Actel's East: I love hafnium.

strategies be doomed to failure?

It is possible that the Intel and AMD strategies of adding more and more cores to PC processors to increase computing performance is a brick wall.

"The challenge of writing software for programming general purpose computing applications is generally recognized in the scientific computing community as the biggest single unsolved, and perhaps unsolvable, computing problem," says Chris Rowen, CEO of Tensilica.

Asked what that means for the business strategies of Intel and AMD trying to get more performance by adding more cores to their x86 architecture chips, Rowen replied: "It means they will find the utilisation will be poor, until we find this hypothetical breakthrough. Until then, the value of the addition of a tenth, or eleventh or fifteenth processor core will be problematical."

Intel's problem and Mentor's problem, and a good many of the industry's problems are caused by the same thing: the heat ceiling imposed by very advanced processing.

"The power per transistor kept going down, but the number of transistors per chip went hugely up, and that causes the power problem," says John East, CEO of Actel.

The heat problem could have been a show-stopper many years ago, but for the emergence of CMOS.

"CMOS was a huge breakthrough 25 years ago. Without CMOS we'd have been through years ago," says East, "since then there have been four breakthroughs: low k, strained silicon, multi-core and high k."



Tensilica's Rowen: Software challenge.

But hafnium compounds, the proposed high k material, won't get the industry back on the old Moore's Law virtuous circle of more density, less power, more performance, less cost.

"I love hafnium. We need it," says East, "but there are four types of power: dynamic power; sub-threshold leakage; gate oxide tunneling, and various miscellaneous power usages. Hafnium only helps with one of the four: gate tunneling oxide."

East's prognosis is gloomy: "With the tools at hand we don't have the capability to lick the power problem. Things will get worse, not better."

Of course all this industry breast-beating is not totally without commercial calculation.

Gavrielov is promoting his FPGAs as an alternative to Asic/ASSP; Vashista is promoting the direct write e-beam approach to Asic manufacturing; Myers is promoting his FPGA verification and prototyping tools; Harding is promoting his risk-sharing business model; Rhines reckons he's got the one and only answer to the impending breakdown in place and route tools; Rowen reckons Tensilica knows more about programming multi-core processors than anyone else; East has the lowest-power FPGA in the industry.

Everyone's good at identifying particular problems within the semiconductor industry when they believe that they have the only solution to solving that problem. That's the way it is, and that's the way it's always been.

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