

ConnX BBE16 (Baseband Engine)

16 MAC/Cycle Scalable, High-Performance DSP

Product Brief

FEATURES

- High-performance DSP with 16 simultaneous 18x18-bit MACs/cycle
- Supports a rich variety of complex arithmetic operations and efficient matrix processing with SIMD acceleration
- Single-cycle radix-4 FFT butterfly, 4 complex tap FIR and 16 real tap FIR operations
- Instruction set optimized for high-performance OFDM and MIMO based communication baseband designs
- Wide vector processing pipeline with up to 8-way SIMD support and 3 issue VLIW for efficient parallel load/store and compute operations
- Single 160b wide vector register file with support for 20b x 8 and 40b x4 vector types
- Dual 128b Load/Store units
- Based on the Xtensa LX platform with rich customization and extension capabilities
- Extensible interfaces with customized FIFO, Port and Lookup interfaces
- Optional acceleration units available:
 - 8-way SIMD integer and fractional divide
 - 4-way SIMD reciprocal square root
 - De-spread (16-way), including Hadamard Transforms

BENEFITS

- Small sized 16MAC DSP core, offering leading performance per area and power
- High I/O throughput with the ability to create custom interfaces to hardwired custom coprocessors and RTL blocks
- Efficient support of scalar vector and matrix operations for real and complex data
- High efficiency allows operation at low clock speeds for low-power designs
- Comprehensive Tensilica multicore tools infrastructure enables use in high-performance cellular base station applications

For Demanding Algorithms for LTE Wireless Handsets and Base Stations

The ConnX BBE16 architecture is optimized for the most demanding wireless DSP tasks, including OFDM algorithms and FFT, FIR, and matrix computation. It is ideal for SOC designs for programmable radio handsets, low-cost femto-cell and pico-cell base stations, micro and macro base stations, digital media broadcast receivers, and multi-format mobile DTV demodulation.

A High-Performance DSP for Wireless Communication

The ConnX BBE16 Baseband Engine is a high performance DSP designed for use in next-generation communication baseband processors in LTE and 4G cellular radios and multi-standard broadcast receivers. The high computation requirements in such applications require new, innovative architectures with a high degree of parallelism and efficient I/O. The ConnX BBE16 meets these needs by combining a 8-way SIMD, 3-issue VLIW processing pipeline with a rich and extensible set of interfaces.

The ConnX BBE16 is built around a core vector pipeline made of 16 18x18b MACs. These multipliers and associated adder and multiplexer trees enable operations such as FFT butterflies, parallel complex multiple operations and signal filter structures. The results of these operations can be full precision or truncated/rounded/saturated and shifted to meet the needs of different algorithms and implementations. High precision is a key factor with ConnX BBE16 and as a result, 512 signed multiplication results can be accumulated without loss of precision.

The instruction set has been optimized for DSP kernel operations such as FFT and FIR as well as matrix multiplies. Acceleration has been added for a wide range of key OFDM wireless functions.

The ConnX BBE16 supports programming in C with a vectorizing compiler. Automatic vectorization of scalar C and full support for vector datatypes allows the development of algorithms without the need to program at the assembly level. Native C operator overloading is supported for natural programming with standard C operators on real and complex vector data types.

Instruction Set

ConnX BBE16 is an option for the popular Xtensa dataplane processor (DPU). The power of the ConnX BBE16 comes from a comprehensive DSP and baseband instruction set.

A wide variety of Load/Store operations supports nine different addressing modes with support for 16b/32b scalar and vector data types. Unaligned Load/Stores with masking deliver full bandwidth Loads and Stores for unaligned data. Vector data management is supported with data packing and shifting.

Multiply operations include complex and scalar 18x18b multiply, multiply-round, multiply-add and multiply subtract functions. Complex-number functions include support for conjugate arithmetic and magnitude operations as well as full precision arithmetic and saturated/rounded outputs. The ConnX BBE16 is capable of performing up to 16 multiplies per operation. BBE16 includes extended precision with guard bits on all register data and full support of double precision data, 40-bit accumulation on all MAC operations without performance



Dataplane. DPU. Differentiate.

Instruction Set (Continued)

penalty. A wide variety of arithmetic, logical and shift operations are supported for up to eight data words per cycle. There is full support for matrix multiplication with acceleration for OFDM matrix operations.

The ConnX BBE16 directly supports single cycle radix-4 and radix-8 butterfly operations enabling efficient high-speed FFT implementations. Support for a single cycle 4-tap FIR filter with complex taps and single cycle 16-tap FIR filter with real taps allows efficient filtering operations. Special instructions supporting radix 3 / 5 FFT are also provided. Symmetric filters on real and complex data at double rate, eg. 32 real taps/cycle.

For further application acceleration optional instruction packages are available offering 8-way SIMD integer and fractional divide, as well as a 4-way SIMD reciprocal square root. There is also a de-spread acceleration package using 16 complex MACs/cycle, that includes Hadamard transforms.

Extensibility

ConnX BBE16 supports custom ports (general purpose wire interfaces) and queue (FIFO) interfaces for efficient connection to coprocessors. These custom interfaces can be defined to match the interfaces of existing RTL hardware blocks. Buffered communication between

two ConnX BBE16s or between a ConnX BBE16 and an RTL block can be automatically implemented using queue interfaces and are fully supported in programming and modeling tools.

Local memories can be connected directly to a ConnX BBE16 DSP using the Lookup interface, bypassing the processor memory bus. This allows efficient implementation of functions that require storage of multiple intermediate datasets. The ConnX BBE16 also can be modified and extended by defining new instructions, registers, and execution units to augment the existing instruction set.

Toolchain

A complete set of tools are available to support the ConnX BBE16. A comprehensive instruction set simulator (ISS) allows developers to quickly simulate and evaluate performance. The fast, functional TurboXim™ simulator option achieves speeds that are 40 to 80 times faster than the ISS for efficient software development and functional verification. System C (XTSC) and C-based (XTMP) system modeling can aid in full-chip simulations.

The toolset includes a high-performance C/C++ compiler with automatic vectorization to support the VLIW pipeline in ConnX BBE16. This comprehensive tool set also includes the linker, assembler, debugger, profiler, an energy estimation tool and graphical visualization tools. All major back-end EDA flows are supported.

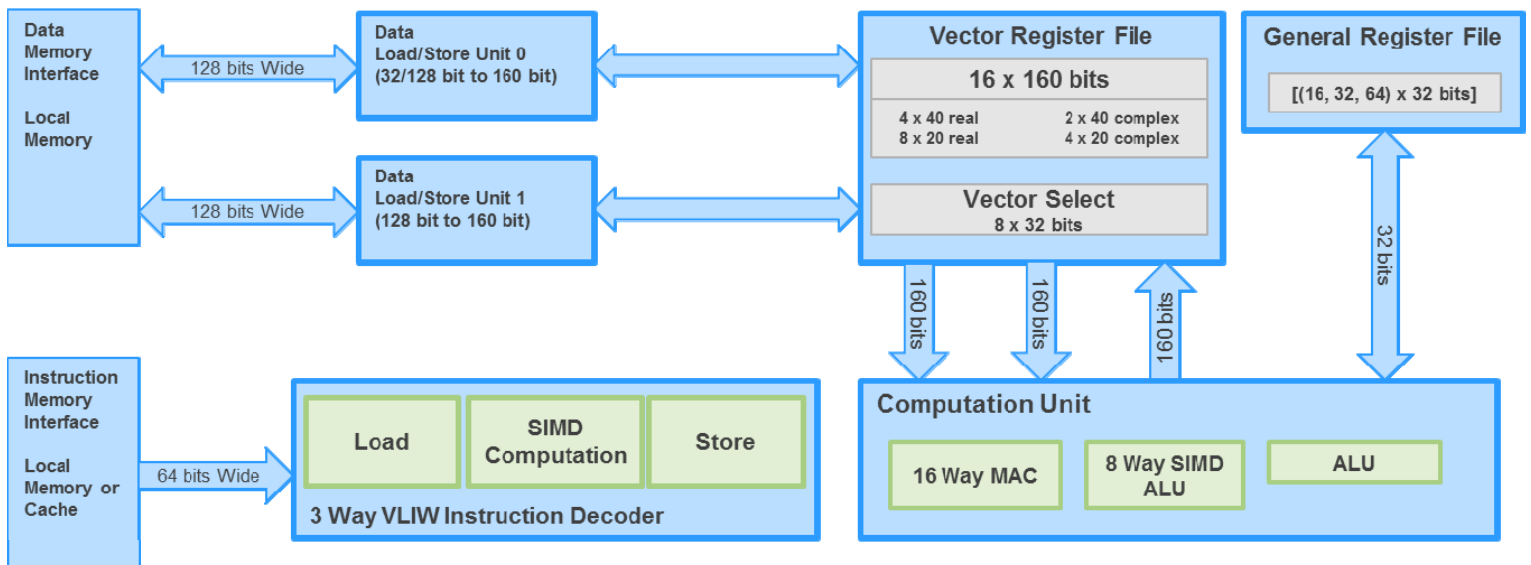


Figure 1. A simplified block structure of the ConnX BBE16 DSP

Tensilica, Inc.

3255-6 Scott Blvd., Santa Clara, CA 95054-3013, USA
Tel: 1-408-986-8000 Fax: 408-986-8919 Website: www.tensilica.com

© July 2011, Tensilica and Xtensa are registered trademarks of Tensilica, Inc.
The Tensilica logo, ConnX, Xplorer and TurboXim are trademarks of Tensilica, Inc. All other trademarks are the property of their respective owners.

