



Success Story



Montego™ OC192c/10G Network Processor/Traffic Manager Relies on Xtensa® Core for Exception Path Processing

B A Y microsystems Bay Microsystems Inc. is a leading provider of highly integrated programmable packet processing devices. These devices are ideally suited for carrier class products such as access concentrators; voice, wireless and xDSL gateways; multi-service switches and routers; cable head ends; and intelligent optical (DWDM, Sonet) transport equipment.

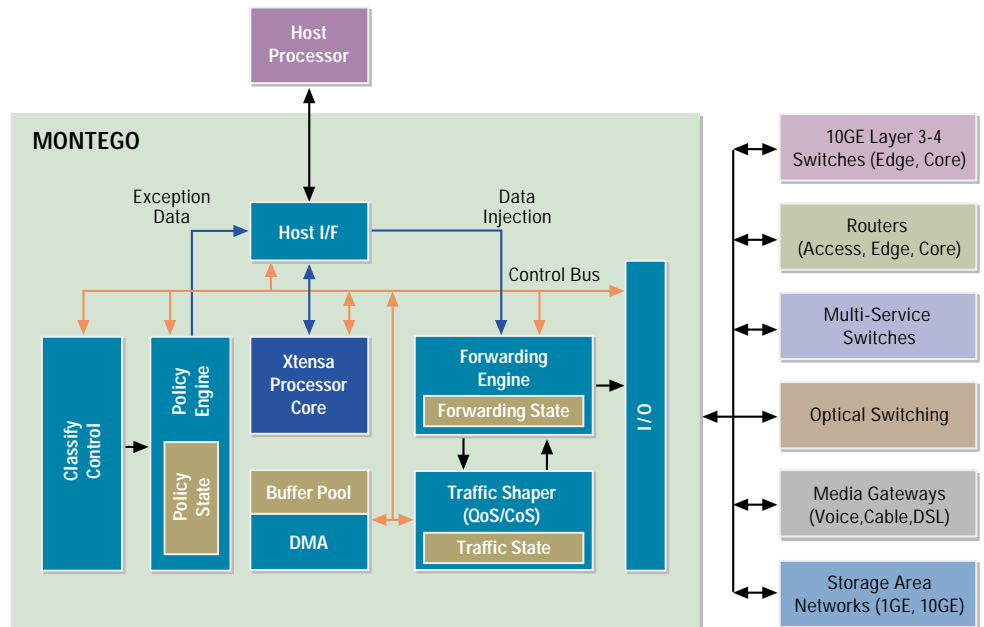
Bay's Internetworking Processor™ (InP™) Family of network processor devices combines scalability, intelligence processing, and high performance in highly integrated solutions. Montego, the flagship product in Bay's InP Family, is the first single chip OC192c/10G network processor, traffic manager, and SAR (Segmentation And Reassembly).

“With its ease of configuration and flexible development tool suite, Tensilica's Xtensa core is the ideal complement to our own programmable pipelined processing elements”, said Chuck Gershman, founder and senior vice president of Bay Microsystems, Inc.

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Bay Microsystems' Design Requirements

To deliver a full-featured, complex and highly integrated network processor and traffic manager (NPU/TM) solution in a timely manner, the Bay team needed a high performance embedded processor core that could easily integrate into Montego and serve as the executive CPU. Also, Montego needed to be fully supported by a world-class



Bay Microsystems' Montego OC192/10G Network Processor and Traffic Manager (NPU/TM) Targets Carrier Markets

Montego integrates NPU/TM functions and SAR in a single chip. The SOC is ideally suited to scale from the access markets to the long-haul markets for carrier class products. Thanks to the Xtensa processor technology, Montego delivers optimum performance for these carrier class products including access concentrators, media gateways, and intelligent optical (SONET) transport equipment.

software environment for immediate application development. Waiting months for software tools for the embedded processor core was out of the question. Bay demanded the best of both worlds for its embedded executive CPU core – a processor core tailored to the exact application needs and a processor with accompanying production-ready, out-of-the-box software tools.

Surmounting Design Barriers

The Bay team was tasked with integrating a system-on-chip (SOC) solution consisting of various building blocks such as a forwarding engine, traffic shaper, SAR, DMA, policy engine, control classification block, I/O interfaces, on-board memory, and an executive CPU for exception path processing. The SOC had to be a scalable, deterministic, single-chip pipelined processor with a simplified programming model and capable of sustaining line rate operation for OC192c/10G applications.

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Solution: Tensilica’s Xtensa Configurable Processor Core

The Xtensa core is the control hub of Bay Microsystems’ Montego chip. Bay engineers configured the Xtensa core and interfaces to optimize the Montego for performance, cost and scalability for network processing applications. Operating at 166MHz, the Xtensa core is the executive processor that interfaces to the various network processing and traffic management building blocks on



Internetworking Development System (IDS)

Complete tool suites combined with a packet processor technology that comprehends the network system application are key ingredients for success. Bay Microsystems has taken this design approach with its Internetworking Development System (IDS). The Xtensa processor generator technology, which includes a complete software tool suite for each processor configuration, helped Bay meet its time to market target for the IDS.

the chip. Bay’s approach allows Montego to deliver the performance of a custom ASIC while offering the flexibility of a programmable network processor.

The Xtensa processor core is designed to freely move along with the rest of the SOC design to the target fabrication process. This feature is in line with Bay’s design approach of having a comprehensive in-house back-end methodology. The Xtensa core ships with a complete set of example scripts that drives various synthesis, verification, layout, and test tools through all the steps necessary to ensure high quality and high performance SOC designs. These deliverables were essential in helping Bay meet its time to market goals.

Comprehensive Software Tool Suite

The Xtensa solution generates a complete software tool suite for each configuration. This tool suite proved beneficial in the development of Bay’s Internetworking Development System (IDS). The IDS is available to Bay Microsystems’ customers as part of a complete development environment, which includes a reference platform, emulators, software tools, and APIs. Months of development time were saved by having key Xtensa software tools available well in advance of the silicon.

Summary

Bay Microsystems had strict time-to-market, performance and cost requirements. Bay’s aggressive design approach and the use of the Xtensa core helped make these goals a reality. With Tensilica’s help, Bay was the first to deliver a 10G single-chip network processor and traffic manager solution and SAR with the launch of Montego.



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