



*The Configurable Processor Company*

# **Next-Generation Audio Engine Technology Preview**

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# Why Do a Next Generation Audio Engine?

## ■ HiFi 1 was already complete

- Success in portable audio and cell phone applications
- Numerous codecs available

## ■ We wanted to do better

- Fewer MHz per codec
- Lower power

***Definition: The HiFi 2 Audio Engine is an Xtensa LX processor with audio specific instructions***

- **General-purpose embedded CPU**
  - Not optimized for high-quality real-time sound processing
- **DSPs**
  - General purpose DSPs use more silicon area than required for audio applications
  - Not a good match for control tasks
- **Hard-wired RTL**
  - Requires one block per audio standard (makes the chip huge)
  - No changes possible without redesigning chip
- **Tensilica's HiFi 1 Audio Engine**
  - Based on Xtensa V architecture
  - Runs AC-3, G.723, G.729AB, MP3, MPEG-2/4 AAC and WMA
  - Designed into:
    - Cell phones
    - Portable Audio Players
  - With new Xtensa LX technology we do better

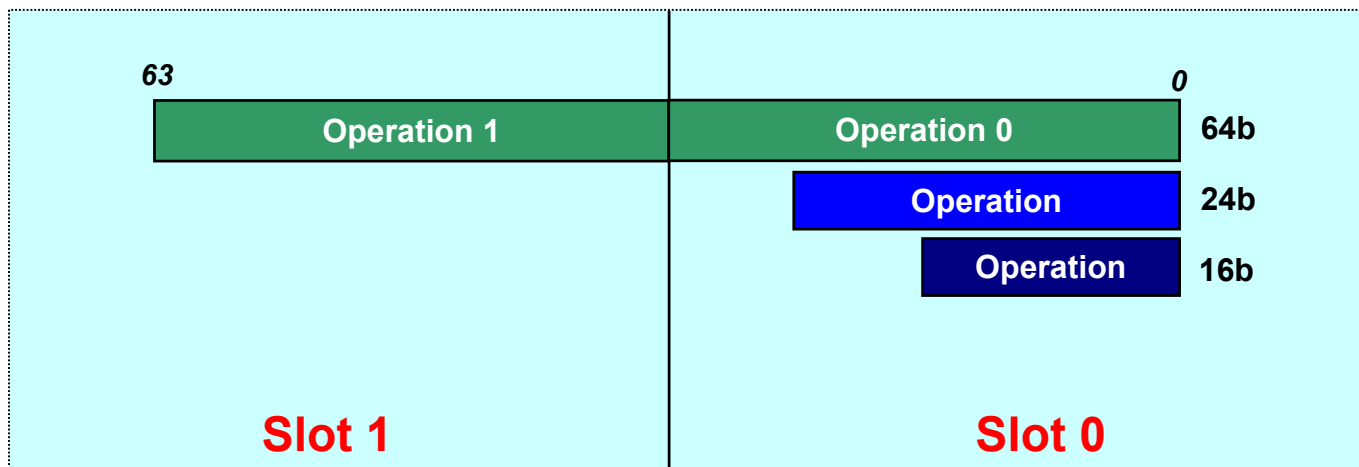
- **Additional codecs**
  - MIDI, 3D audio, aacPlus
- **Even lower power**
- **More regular ISA than HiFi 1**
  - Makes for an easier programming model
- **Same performance at a lower clock rate**
- **Higher maximum clock rate**
  - More headroom for additional tasks
  - Processor can run multiple codecs simultaneously

## ■ HiFi 2 has more than 300 audio-specific instructions

- Dual multiply / accumulate
  - Each supports 24 x 24 bits and 32 x 16 bits
  - Both multipliers operate every cycle
- Huffman encode / decode and bit stream support
  - Streams interleave coded / uncoded items
- Convert / round / truncate instructions
- Two special audio register files with multiple data types
  - 8 x 48 bits (each holds two 24-bit values)
  - 4 x 56 bits
- Two way SIMD arithmetic and boolean operations on 24-bit or 16-bit data

# HiFi 2 Instruction Format

*Dual Issue 64-bit (FLIX) or Single Issue 24/16-bit Instructions*

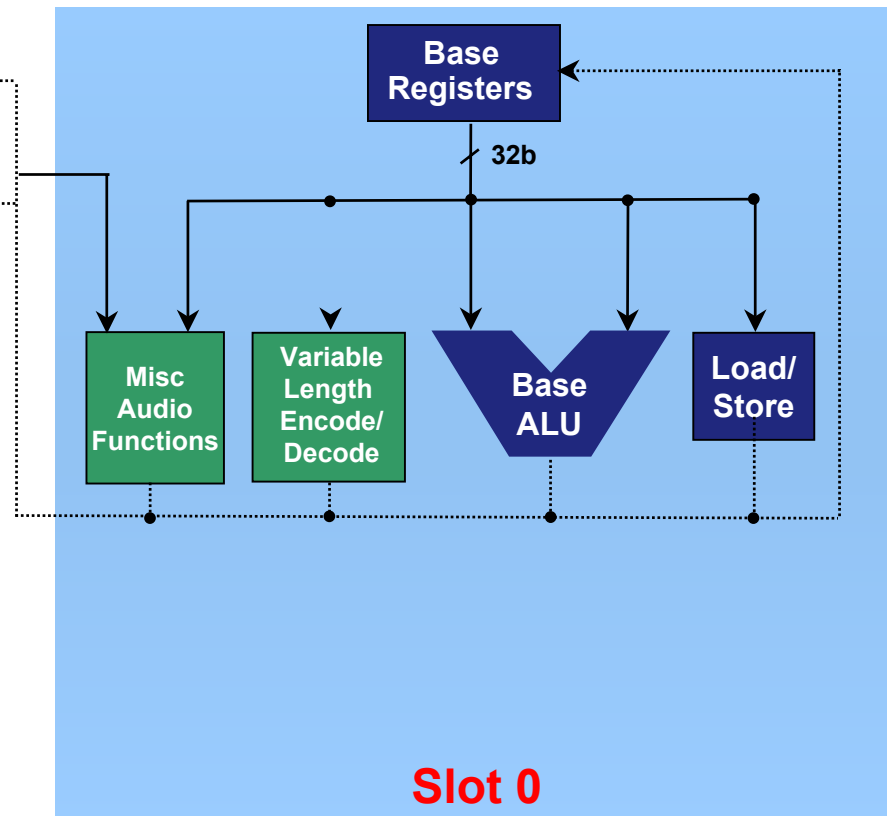
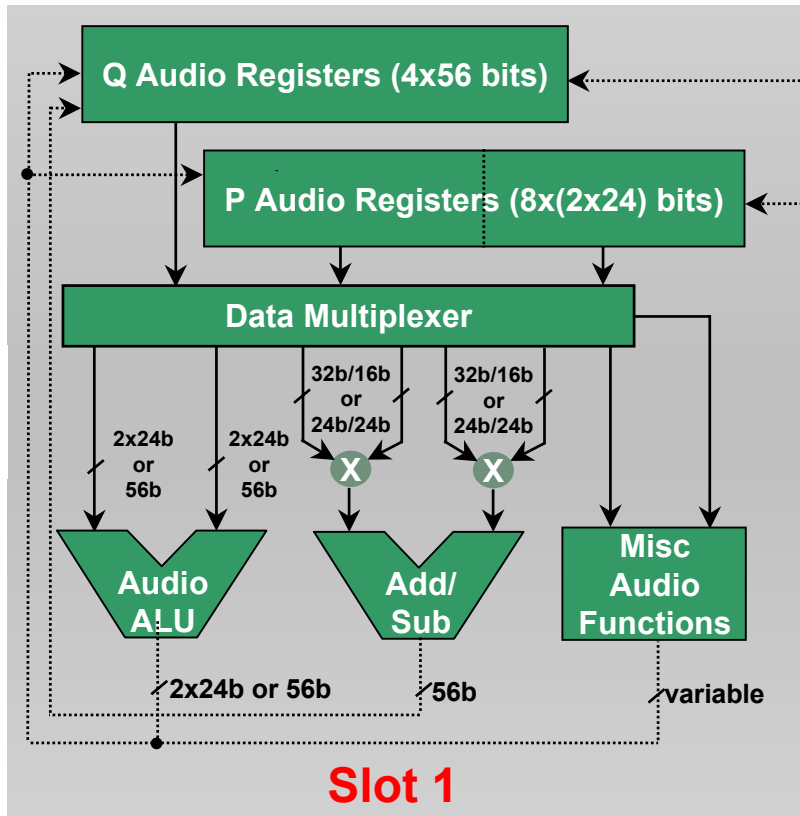


- HiFi2 Audio Instructions
- Base/HiFi2 Audio Instructions
- Base LX Instructions

**Multiply and Audio  
ALU Instructions**

**Load/store, Huffman  
instructions**

# HiFi 2 Block Diagram



■ HiFi 2 Audio Engine Hardware

■ Base Xtensa LX Configuration



# Instruction Set Summary

Operations	Slot	Description
<b>Load/Store Operations</b>		
AE_LP16F.I, AE_LP16X2F.I, AE_LP24.I, AE_LP24F.I, AE_LP24X2.I, AE_LP24X2F.I (.X .IU .XU)	0	Load a single or a pair of 16- or 32-bit values as two 24-bit (1.23) signed fixed-point fractions in AE_PR. Addressing through an immediate or index offset, with without address register update.
AE_LQ32F.I, AE_LQ56.I (.X .IU .XU)	0	Load a 32- or 64-bit value as a 56-bit (9.47) signed fixedpoint fraction in AE_QR.
AE_SP16F.L.I, AE_SP16X2F.I, AE_SP24S.L.I, AE_SP24F.L.I, AE_SP24X2S.I, AE_SP24X2F.I (.X .IU .XU)	0	Store a single or a pair of 24-bit (1.23) signed fixed-point fractions from AE_PR as 16- or 32-bit values. Addressing through an immediate or index offset, with or without address register update.
AE_SQ32F.I, AE_SQ56S.I (.X .IU .XU)	0	Store a 56-bit (9.47) signed fixed-point fraction from AE_QR as a 32- or 64-bit value.
<b>Multiply/Accumulate Operations</b>		
AE_MULf P24S.LL (.LH .HL .HH), AE_MULaf P24S.LL (.LH .HL .HH), AE_MULZaaf P24S.HH.LL (.HL.LH), AE_MULAaf P24S.HH.LL (.HL.LH)	1	24x24- to 56-bit signed single and dual MAC, no saturation.
AE_MULaf S56P24S.LL (.LH .HL .HH)	1	24x24- to 56-bit signed single MAC with 56-bit accumulator saturation.
AE_MULFS32P16S.LL (.LH .HL .HH), AE_MULa FS32P16S.LL (.LH .HL .HH)	1	16x16- (1.15) to 32-bit (1.31) signed fixed-point fraction single MAC with 32-bit product and accumulator saturation.
AE_MULf Q32P16S.L (.H), AE_MULaf Q32P16S.L (.H), AE_MULf Q32P16U.L (.H), AE_MULaf Q32P16U.L (.H), AE_MULZaaf Q32SP16S.LL (.LH .HH) AE_MULZaaf Q32SP16U.LL (.LH.HH)	1	32x16- to 56-bit single and dual MAC, no saturation. Accumulate Operations

# Instruction Set Summary

Operations	Slot	Description
<b>Arithmetic Operations</b>		
AE_MINP24S, AE_MINBP24S, AE_MAXP24S, AE_MAXBP24S, AE_MINQ56S, AE_MINBQ56S, AE_MAXQ56S, AE_MAXBQ56S	1	Minimum and maximum on AE_QR and element-wise on AE_PR, with and without booleans.
AE_ADDP24, AE_SUBP24, AE_NEGP24, AE_ABSP24, AE_ADDQ56, AE_SUBQ56, AE_ABSQ56, AE_NEGQ56	1	Add, subtract, negate and absolute value on AE_QR and element-wise on AE_PR. Each operation has a version that performs signed saturation on the result.
AE_LTP24S, AE_LEP24S, AE_EQP24, AE_LTQ56S, AE_LEQ56S, AE_EQQ56	1	Signed comparison on AE_QR and element-wise on AE_PR.
<b>Shift Operations</b>		
AE_SRLIP24, AE_SRAIP24, AE_SLLIP24, AE_SLLISP24S, AE_SRLSP24, AE_SRASP24, AE_SLLSP24, AE_SLLSSP24S	1	Element-wise shift on AE_PR, with and without signed saturation; variable (from state) or immediate shift amount.
AE_SRLIQ56, AE_SRAIQ56, AE_SLLIQ56, AE_SLLISQ56S, AE_SRLAQ56, AE_SRAAQ56, AE_SLLAQ56, AE_SLLASQ56S, AE_SRLSQ56, AE_SRASQ56, AE_SLLSQ56, AE_SLLSSQ56S	0	Shift on AE_QR, with and without signed saturation; variable (from AR or state) or immediate shift amount.
<b>Bit Stream and Variable-Length Encode/Decode Operations</b>		
AE_SHA32	Inst	Swap the two half words of an AR register.
AE_VLDSHT, AE_VLDL16C, AE_VLDL16T, AE_VLDL32T	Inst	Variable-length decode with 16- and 32-bit entry codebook tables.
AE_VLEL16T, AE_VLEL32T, AE_VLES16C	Inst	Variable-length encode with 16- and 32-bit entry codebook tables.
AE_LB, AE_LBI, AE_LBK, AE_LBKI	Inst	Look-ahead bits in the input bit stream.
AE_DB, AE_DBI	Inst	Discard bits from the head of the input bit stream.
AE_SB, AE_SBI, AE_SBF	Inst	Store bits to the output bit stream.



# Instruction Set Summary

Operations	Slot	Description
<b>Miscellaneous Operations</b>		
AE_ANDP48, AE_NANDP48, AE_ORP48, AE_XORP48, AE_ANDQ56, AE_NANDQ56, AE_ORQ56, AE_XORQ56	1	Bitwise logical operations on AE_PR and AE_QR.
AE_NSAQ56S	0	56-bit signed normalization shift amount on AE_QR.
AE_SATQ48S	1	56- (9.47) to 48-bit (1.47) signed fixed-point fraction saturation on AE_QR.
AE_ROUNDSP16SYM (ASYM), AE_ROUNDSP24Q48SYM (ASYM), AE_ROUNDSP16Q48SYM (ASYM), AE_ROUNDSP32SYM (ASYM)	1	Symmetric and asymmetric rounding on AE_PR and AE_QR
AE_TRUNCPC24Q48X2, AE_CVTQ48P24S.L (.H), AE_TRUNCPC16, AE_TRUNCQ32	1	Truncate and convert fractions between AE_PR and AE_QR.
AE_TRUNCAC32Q48, AE_TRUNCAC16P24S.L (.H), AE_TRUNCPC24A32X2, AE_CVTA32P24.L (.H), AE_CVTP24A16X2, AE_CVTP24A16X2.LL (.LH, .HL, .HH) AE_CVTQ48A32S, AE_MOVPA24X2, AE_MOVAP24S.L (.H)	0	Truncate and convert fractions between AE_PR/AE_QR and AR.
AE_MOVP48, AE_MOVQ56	0,1	Unconditional moves on AE_PR and AE_QR.
AE_MOVTP48, AE_MOVFP48, AE_MOVTP24X2, AE_MOVFP24X2	1	Conditional moves on AE_PR.
AE_MOVTQ56, AE_MOVQ56	0	Conditional moves on AE_QR.
AE_SELPC24.LL (.LH .HL .HH)	1	Element-wise AE_PR selection/permutation.
AE_ZEROP48, AE_ZEROQ56	1	Zero an AE_PR or AE_QR register.

## ■ HiFi 2 MAC alternatives

- **24 x 24 bits**
- **32 x 16 bits**
- 32 x 32 bits
- Single or **dual multiplier**

## ■ Memory bandwidth:

- **64-** vs. 128-bit bus requirement
- **One** vs. two load/store units
- **Bandwidth >2 GB/sec**

*Implemented features shown in green*

	Maximum clock rate (MHz)*	Gates*
Single 24x24-bit MAC	299	88,569
Dual 24x24-bit MAC	289	100,860
Dual MAC supporting 24x24 and 32x16	284	101,408
Dual MAC supporting 24x24, 32x16 and single 32x32	270	110,012

\* Based on TSMC 0.13 um LV, Artisan library

## ■ Six weeks from concept to first delivered implementation

- Developed with customer input
- Processor core RTL
- Complete software-development tools
  - C/C++ compiler
  - Debugger
  - Linker
  - Simulator
  - Assembler
  - Profiler

# Selected Codec Preliminary Specs

Codec	Worst Case Required MHz	Worst Case MHz measured for
HiFi 2 MP3 Decoder	13-15	48 kHz / 128 kbps (stereo)
HiFi 1 MP3 Decoder	18	48 kHz / 320 kbps (stereo)
HiFi 2 MP3 Encoder	38-40	44.1 kHz / 128 kbps (stereo)
HiFi 1 MP3 Encoder	65	48 kHz / 128 kbps (stereo)
HiFi 2 AAC-LC Decoder	11-12	48 kHz / 128 kbps (stereo)
HiFi 1 AAC-LC Decoder	26	48 kHz / 128 kbps (stereo)
HiFi 2 AAC-LC Encoder	35-38	44.1 kHz / 128 kbps (stereo)
HiFi 1 AAC-LC Encoder	85	48 kHz / 192 kbps (stereo)
HiFi 2 WMA Decoder	16-18	32 kHz / 22 kbps (low-rate, stereo)
HiFi 1 WMA Decoder	30	32 kHz / 22 kbps (low-rate, stereo)

- **Reduced required MHz for all codecs**
  - Encoders improved by >40%
- **More regular programming model**
- **Gate count comparable to HiFi 1**
- **Higher maximum clock rate than HiFi 1**