



The Engine of SOC Design

Achieving Very High-Performance Processing in Networking Data Plane

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TechOnline Webinar

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Why You Want to Listen – What We'll Discuss

- **Advantages of processors in the data plane**
- **Limitations of traditional processors**
- **Advantages of Xtensa processor**
 - A different kind of processor – you can optimize it
 - Achieves high performance and I/O throughput
- **Examples:**
 - Xtensa in control plane
 - Xtensa in data plane

■ Line rates are rising

- 1GbE, 10GbE, 40GbE, OC-192, OC-768...

■ Evolving protocol standards

- FiberChannel over Internet Protocol
- Encapsulating SCSI over TCP/IP networks (iSCSI)
- Media content: IGMP version 2 & 3

■ High-value Internet services

- VoIP (Voice over IP)
- IPTV (Internet Protocol Television)
- Video on demand

Data Plane Programmability

- Support evolving protocols
- Build multi-protocol engines
- Support multiple markets and emerging high-value services

Flexibility

Processor-based Task Engine

- Less or no hardwired logic in data plane
- Fix bugs post-silicon – in software

Reduce Verification Effort/Time

Easy to add more processors

- Support increasing complexity
- Support higher number of packet streams

Scalability

- **Networking thrives on speeds and feeds**
- **Traditional processors provide neither performance nor throughput**

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Limitation 1

Lack Sufficient I/O Capability

- System-bus bottleneck
- 32-bit Load/Store constraint

Limitation 2

Not Optimized for Networking

- Rely on higher MHz for higher performance
- No networking and algorithm-specific acceleration

Xtensa Processor: Powerful Building Block for Networking SOCs

Xtensa Configurable Processors

Configuration options

- Mul16x16
- Floating-point unit
- Barrel Shifter
- Zero overhead looping

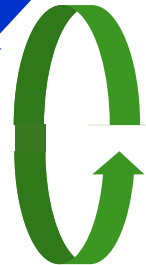
Extend processor

- Add register files
- multi-cycle exec units
- VLIW data path
- GPIO, FIFO interfaces

**Xtensa
Processor
Generator**



Iterate
in minutes



Base CPU		OCD
Extended Data path	Cache	Timer
Extended Registers		FPU

**Application-
optimized
processor**

RTL, EDA scripts,
test benches



**Automatically
generated
Software Tools**

C/C++ compiler
Debugger,
Simulators, RTOSes

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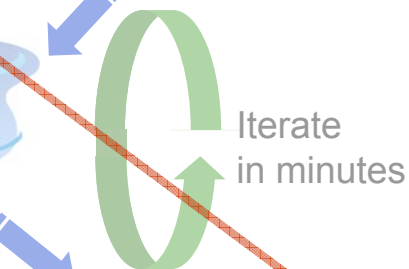
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Configurability

Base processor is 20K gates

Choose features you need

- Mul16x16
- Mul32x32
- Floating-point unit
- MMU
- HiFi 2 Audio Engine
- Vectra LX DSP

Select interface/memory sizes

- 32 ▾ Number of Registers
- 32 ▾ Width of Local Instruction Memory Interface
- 128 ▾ Width of Local Data Memory Interface
- 32 ▾ Width of PIF System Interface

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Extensibility

- ▀ **Add application-specific instructions and data paths**
 - Register files
 - Multi-cycle
 - SIMD function units
 - Multi-issue VLIW data path, etc.
 - GPIO, FIFO, lookup interfaces
- ▀ **Create optimized task engines**

Xtensa Processor: Powerful Building Block for Networking SOCs

Xtensa Configurable Processors

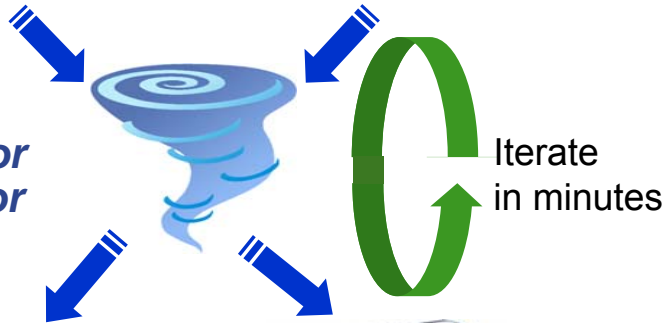
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Automated Processor Generation

- Xtensa Processor Generator**
 - RTL, EDA scripts
 - Complete software tool chain
- Inserts clock gating**
 - Extremely fine grain
- Optimized implementation of
designer-defined data path**

Xtensa Processor: Powerful Building Block for Networking SOCs

Xtensa Configurable Processors

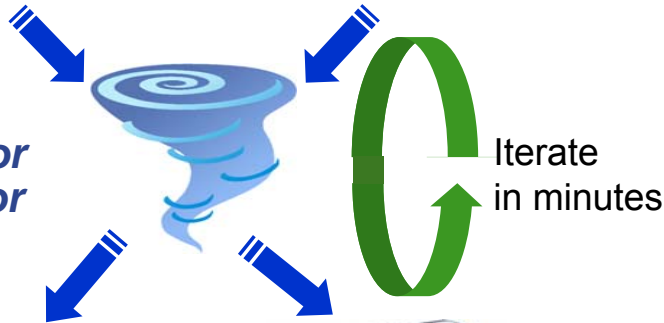
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Automatic Generation of SW Tools

- Program in C/C++ -- no assembly coding required
 - Compiler schedules new instructions and register files
- ISS simulates new instructions
- Debugger displays new registers

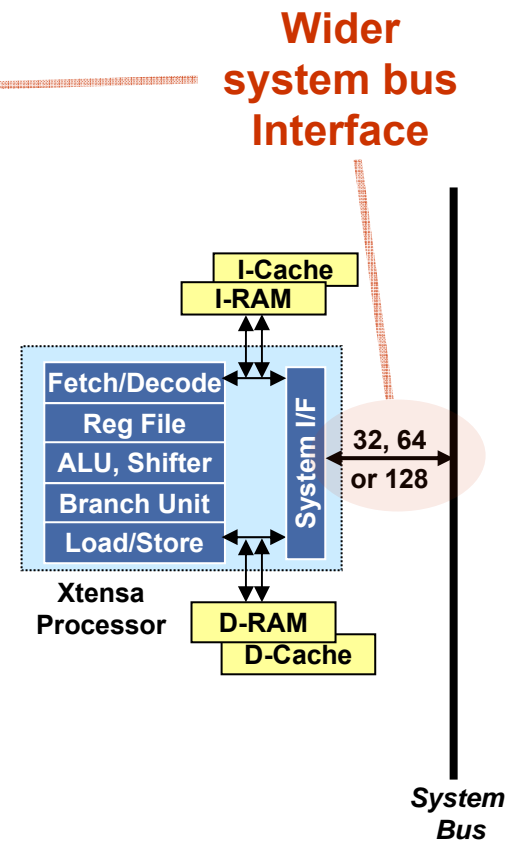
Xtensa Overcomes Limitations of Traditional Processors

Tackling the Data Throughput Bottleneck

Xtensa orders of magnitude higher than conventional CPUs

Overcoming Limitation 1

■ Configure 32, 64, or 128-bit system interface on Xtensa
 + Dual load/store units



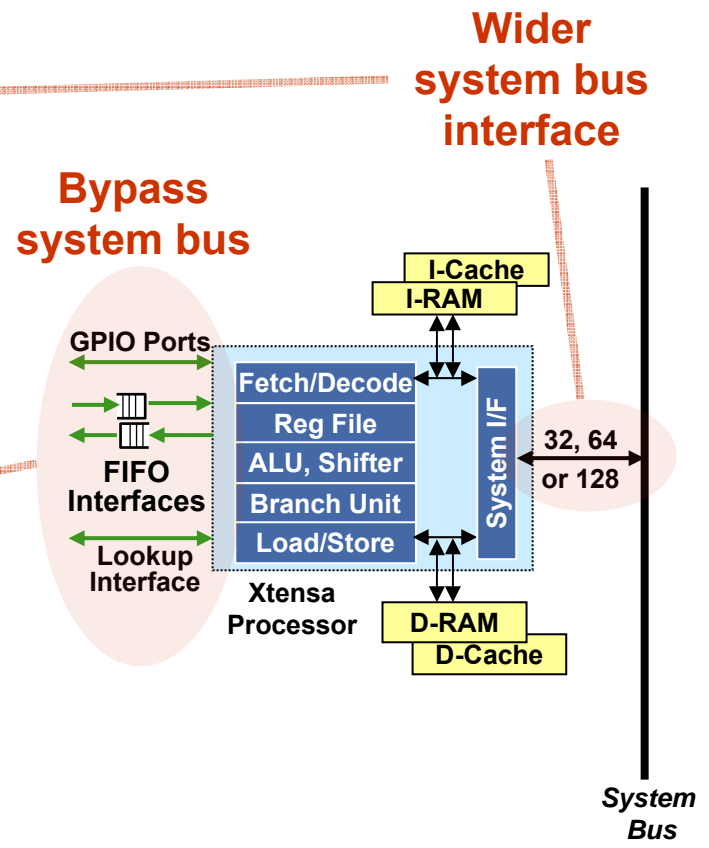
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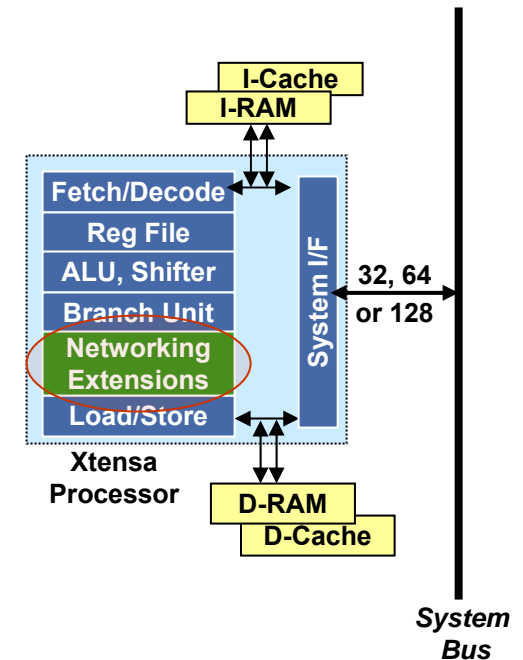
- Bypass system bus → direct interfaces
- Interfaces wired directly into computation units
 - GPIO ports
 - FIFO interfaces
 - Lookup interfaces
- Enables very high throughput
 - Up to 1024 interfaces -- 1024 bits each



Overcoming Limitation 2

■ Add application-specific instructions to Xtensa

- Build optimized networking task engine
- Lower MHz → lower power



Overcoming Limitation 2

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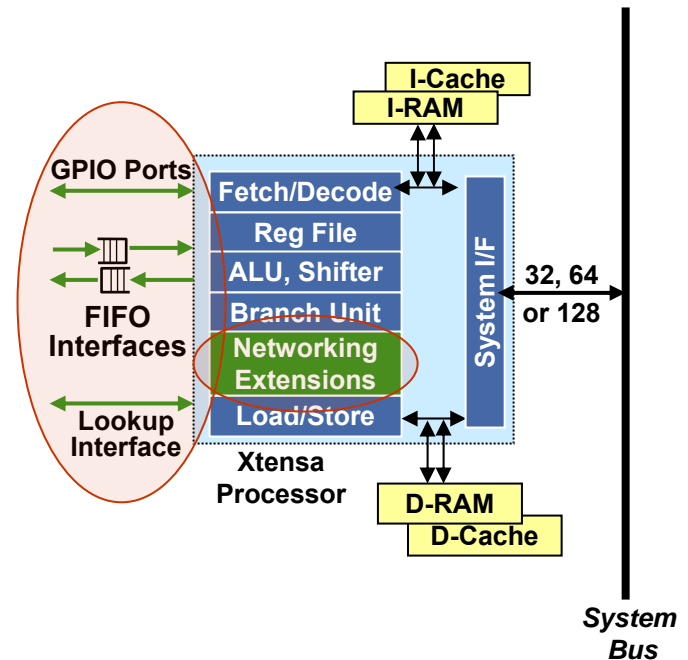
Networking-specific processing units

+

FIFO, Lookup, GPIO Interfaces

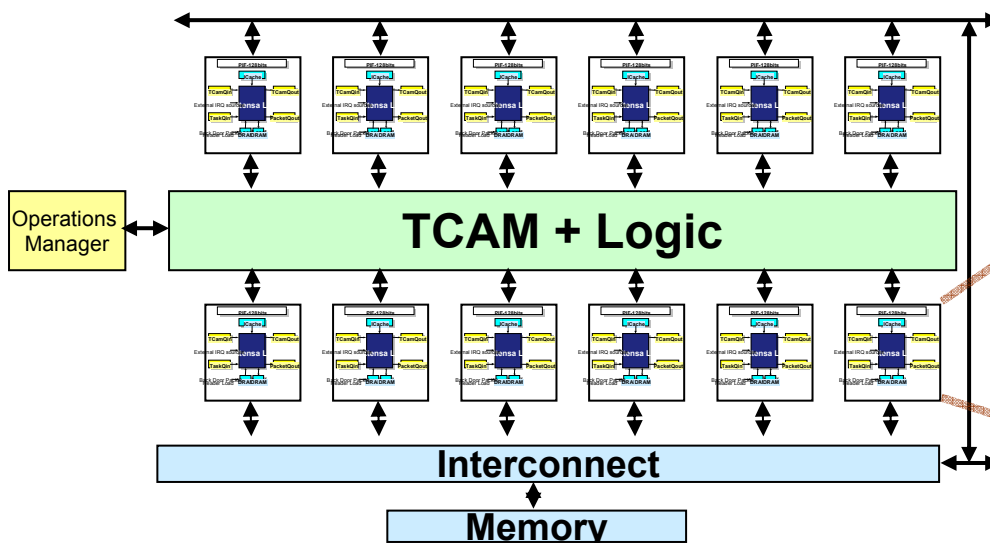
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Very high performance & throughput

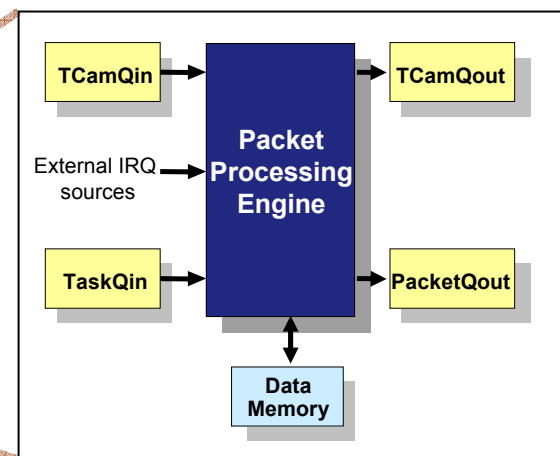


- ▀ **Use processors instead of RTL**
 - Data flow does not change
- ▀ **Add processors as complexity scales**
- ▀ **Each processor is networking task engine**

Packet Classification Example



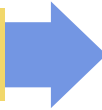
Packet Processing Engine





Advantages: Tensilica-based Networking Engines

High Flexibility of Tensilica Processors



RTL-like Performance

- **Xtensa-based data path ↔ hardwired RTL**
 - Easy to specify complex, multi-cycle operations

High Flexibility of Tensilica Processors →

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Processor-based Task Engine →

Lower Implementation & Verification Effort

- **Specify only functional behavior of data path**
 - No detailed RTL implementation required
- **Verify only functional behavior**
 - Automatic generation of pre-verified RTL



Advantages: Tensilica-based Networking Engines

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Programmability

Lower Verification Effort

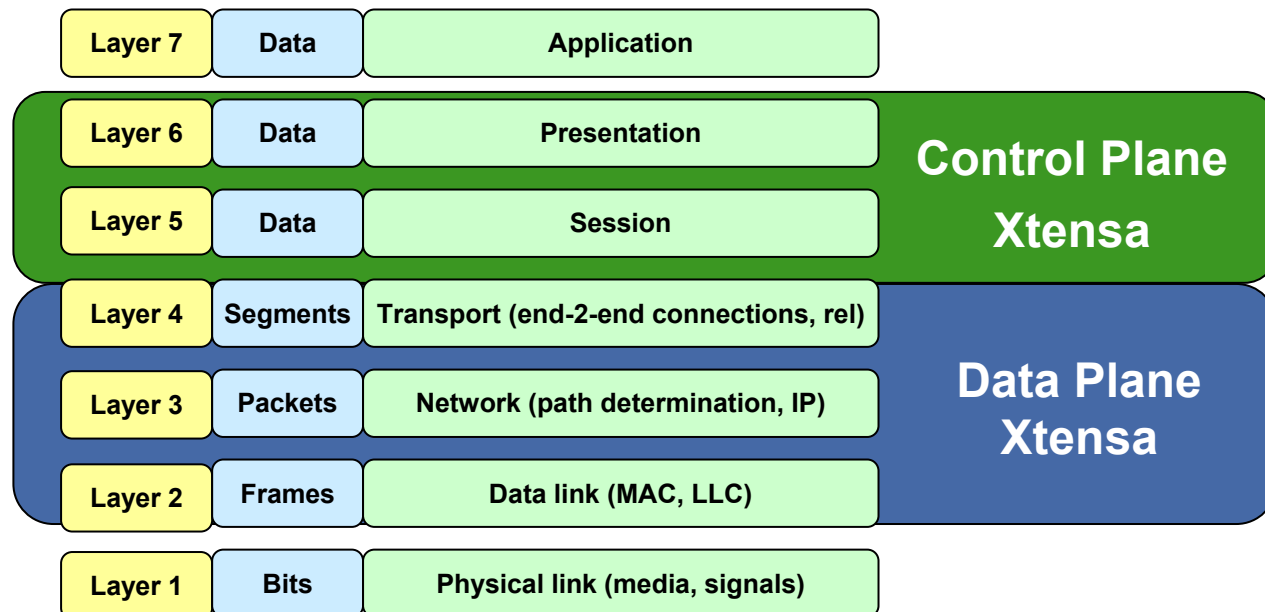
- **Implement control FSM as software on processor**
- **90% of RTL bugs in control logic**
 - Control logic \leq 10% of total logic

Use of Xtensa in Networking

Dual Use: Control and Data Plane

Xtensa in use in OSI layer 2, 3 and 4 applications

- TOE-engines, MACs, bridging, routing
- Packet classification, AAL5 SAR, and IPSEC (3DES)
- Network speeds from DS-1 to 96 Gb/s



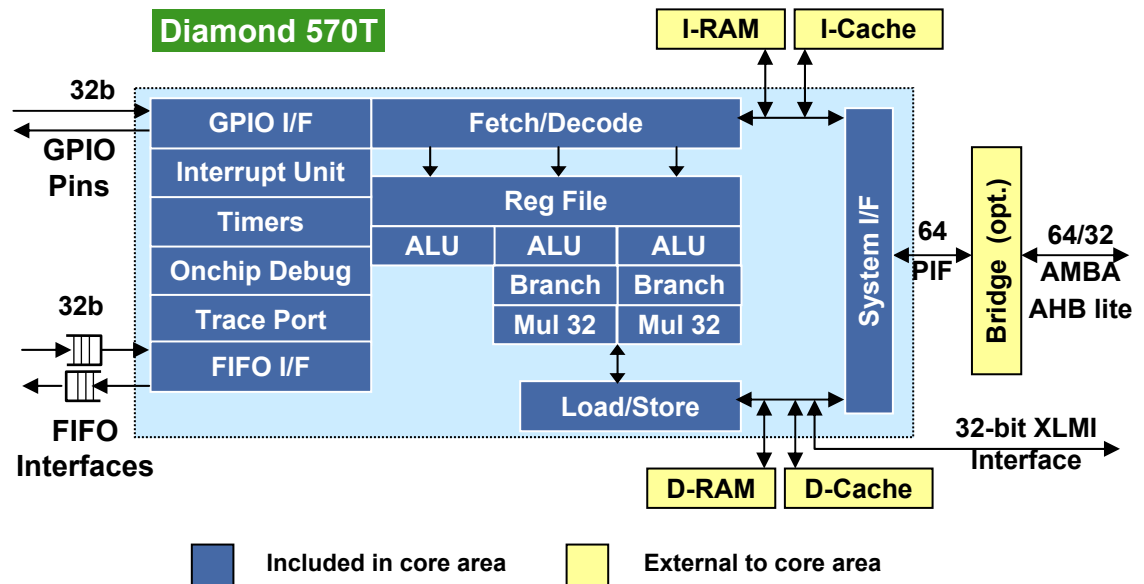
Control Plane Example



Tensilica Diamond 570T

An Instance of a High-Performance Xtensa

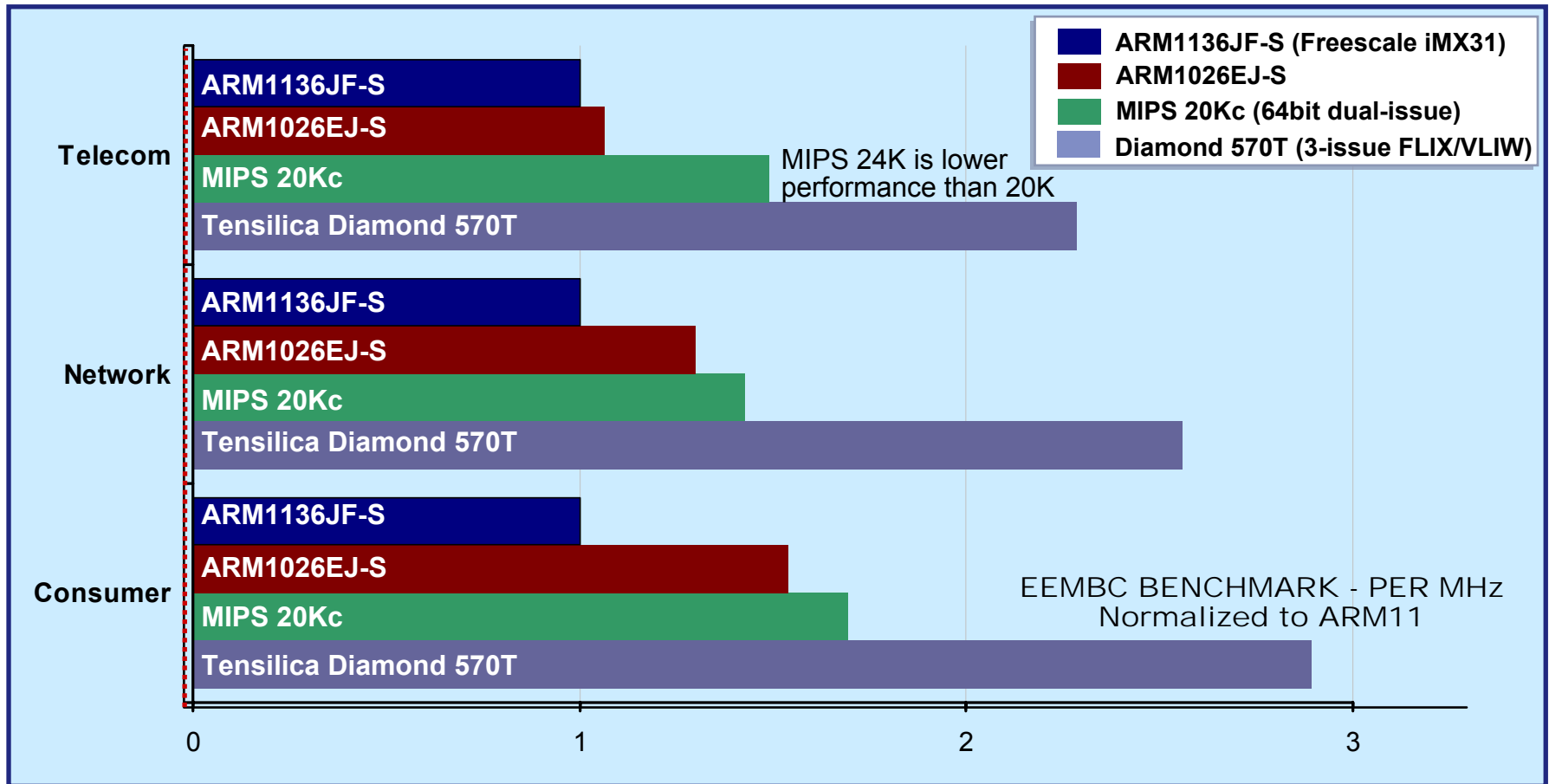
- 3-issue VLIW CPU
- No C code modification required
 - Compiler automatically packs VLIW instructions
- Two SIMD 32x32 MACs
- 2x 32-bit I/O ports & FIFO interfaces
- Very high performance





Diamond 570T is Highest Performance General-Purpose CPU - EEMBC

Diamond 570T is 2.3 to 2.9x higher performance/MHz than ARM11



All scores are Simulations of Licensable cores.

All scores are EEMBC/ECL Certified. All scores "out of the box"

Per-MHz certified benchmark scores normalized to ARM = unit score of 1 for suitability in graphing.

Tensilica Diamond 570T

2x Performance of ARM11

2.3x Performance => 50% Higher Effective Frequency

	ARM1156T2-S	Diamond 570T	ARM1136J-S
AREA and PERFORMANCE	1/2 the die area, much more efficient/Mhz		
Max Frequency (90G) Sage-HS library, optimized for speed	620	892 (EEMBC equivalent freq) Actual = 388 Mhz	620
Dhrystone MIPS/MHz	1.20 (est.)	1.52	1.20
Area (90G, pre-layout) Sage-HS library, optimized for speed	1.75 mm ²	0.6 mm ²	1.8 mm ²
POWER	Much lower power consumption		
mW per MHz (90G) Sage-HS library, optimized for speed	0.42	0.13	0.37
mW for the same performance	260 mW @ 620 MHz	50 mW @ 388 MHz	229 mW @ 620 MHz
FEATURES	More features		
Instruction width	16/32 bit	16 / 24 / 64b 3-issue	16/32 bit
High throughput FIFO Interfaces	No	2 x 32 I/O FIFO interfaces	No



Tensilica Diamond 570T

1/3rd Area of ARM11

1/3rd the Area

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Tensilica Diamond 570T

Higher Performance at Lower Cost

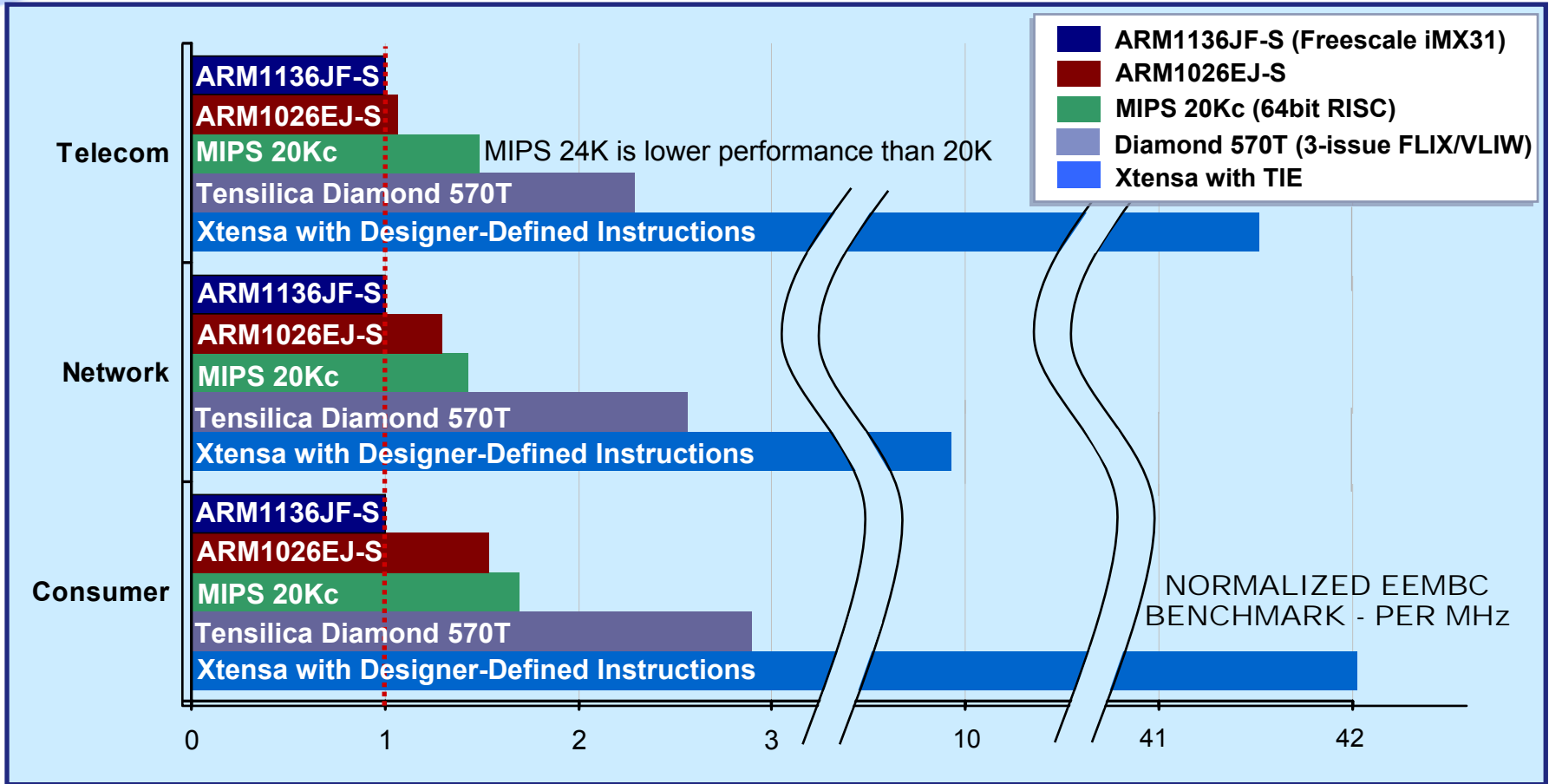
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Data on ARM products taken from ARM public website and product information flyers, May 2007

Diamond Standard Core data are subject to change. All speed, power, area metrics are subject to variation based on user's design tools, libraries, and fab choices

Application-Optimized Xtensa Blows Away the Competition

EEMBC Benchmark Results



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Competitive Data as of June 2006. Source: www.eembc.org

Data Plane Examples Using Xtensa Processors

- **IPSEC 3DES**
- **Packet Classification**



Data Plane Example #1: IPSEC 3DES

- **3DES computationally intensive at bit level**
- **1000's of instructions per 3DES cipher-block**

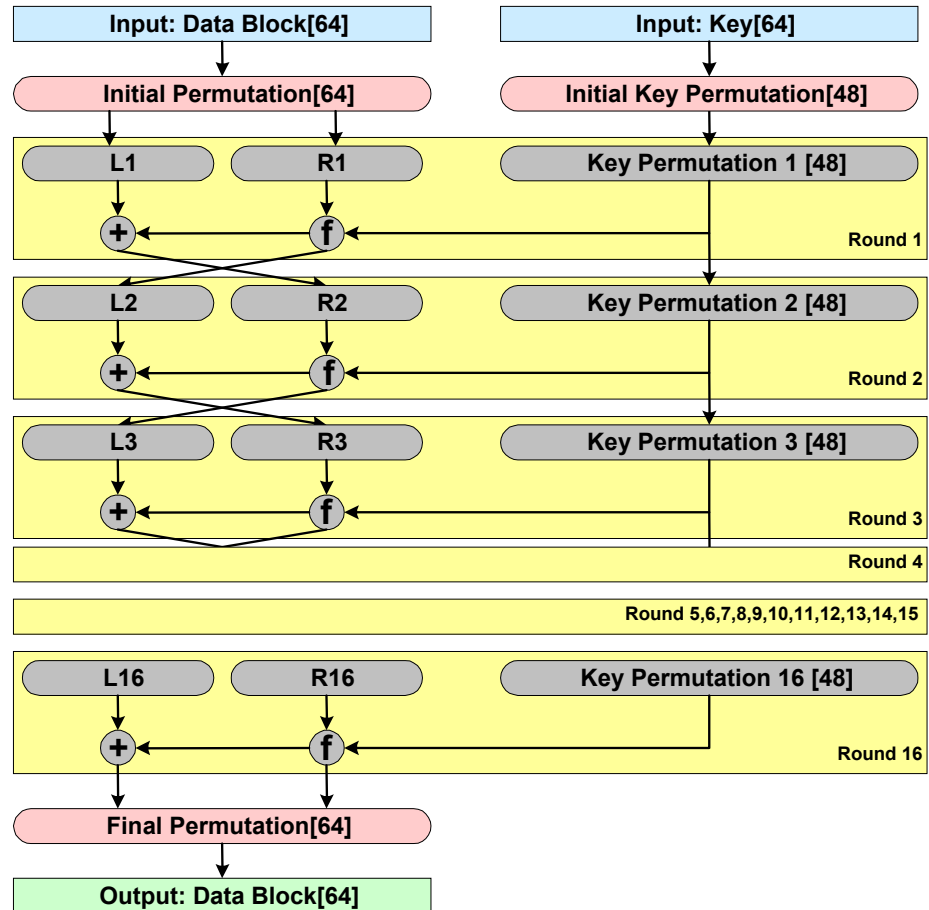
- **3DES computationally intensive at bit level**
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- **With instruction extensions**
 - One cycle for two DES rounds
 - 8 cycles for complete single DES (16 rounds)
 - 24 cycles per 3DES cipher-block
 - i.e. 24 instructions
 - Code density increases
 - New instructions become native to Xtensa core

- ▀ **Single DES block**
- ▀ **Each round contains**
 - Two 32-bit values L,R
 - 32-bit exclusive-or (+) operations
 - Bit scrambler (f)
 - Key permutation

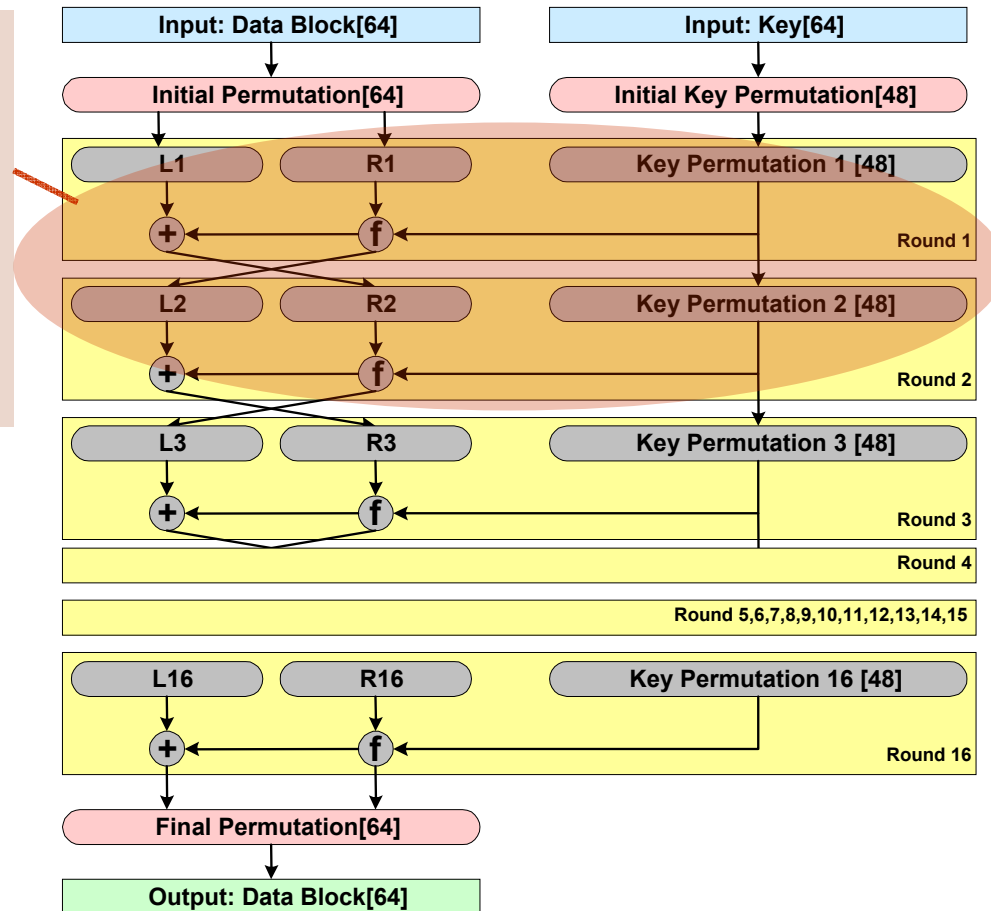
Single DES Block Diagram



One new (TIE) instruction

- 2-rounds in one cycle
- Parallel computation
 - XOR (+)
 - Scrambler (f)
 - Key Permutation
- 64-bit processing

Single DES Block Diagram



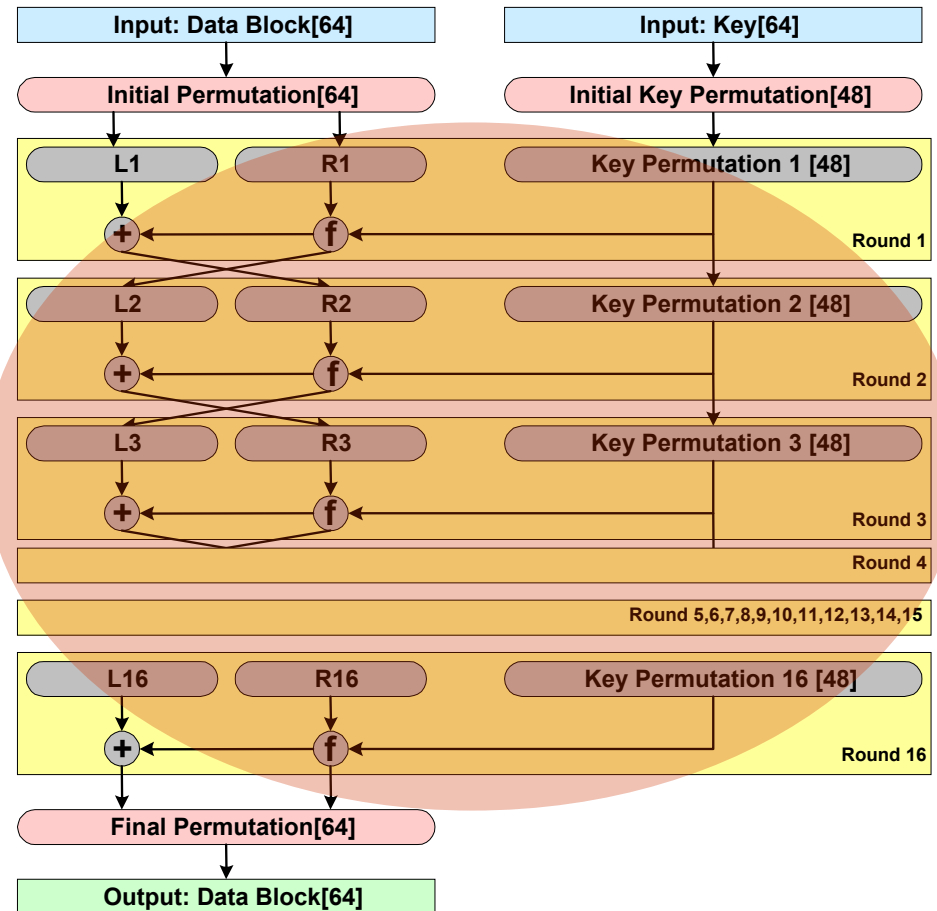
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- 64-bit processing

8 instructions to do 16 rounds

8 cycles per DES cipher-block

Single DES Block Diagram



■ Performance (250MHz TSMC 130nm LV)

- 8-clocks per DES cipher-block
 - Data rate: 31.250 million DES blocks/second (2 Gb/s data rate)
- 24-clocks per 3DES cipher-block
 - Data rate: 10.416 million 3DES blocks/second (666 Mb/s data rate)

■ 64-bit local memory interfaces

- Data remains in memory local to processor

■ Single Xtensa processor for encryption and decryption

- Xtensa 3DES performance rivals RTL

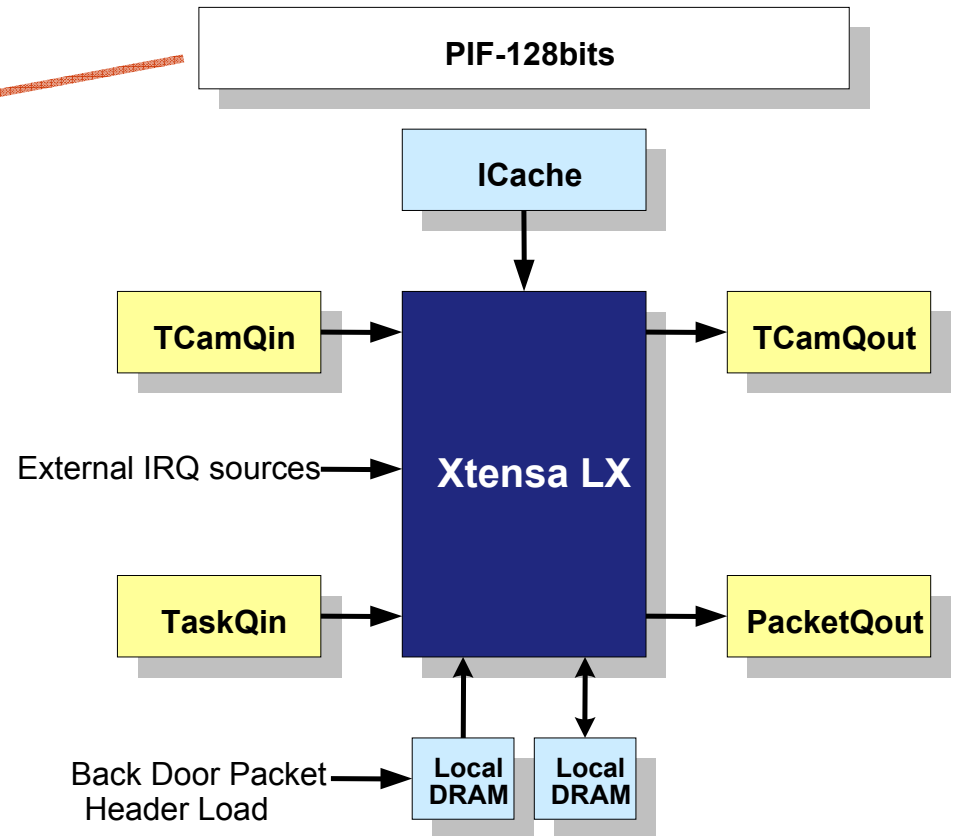
■ Requirement: 20Gbps Ethernet line rate

- Minimum packet size of 84 bytes
 - 64 bytes packet, 20 bytes overhead
- Approx 29.6M packets/sec

■ Solution: Multiple processor architecture

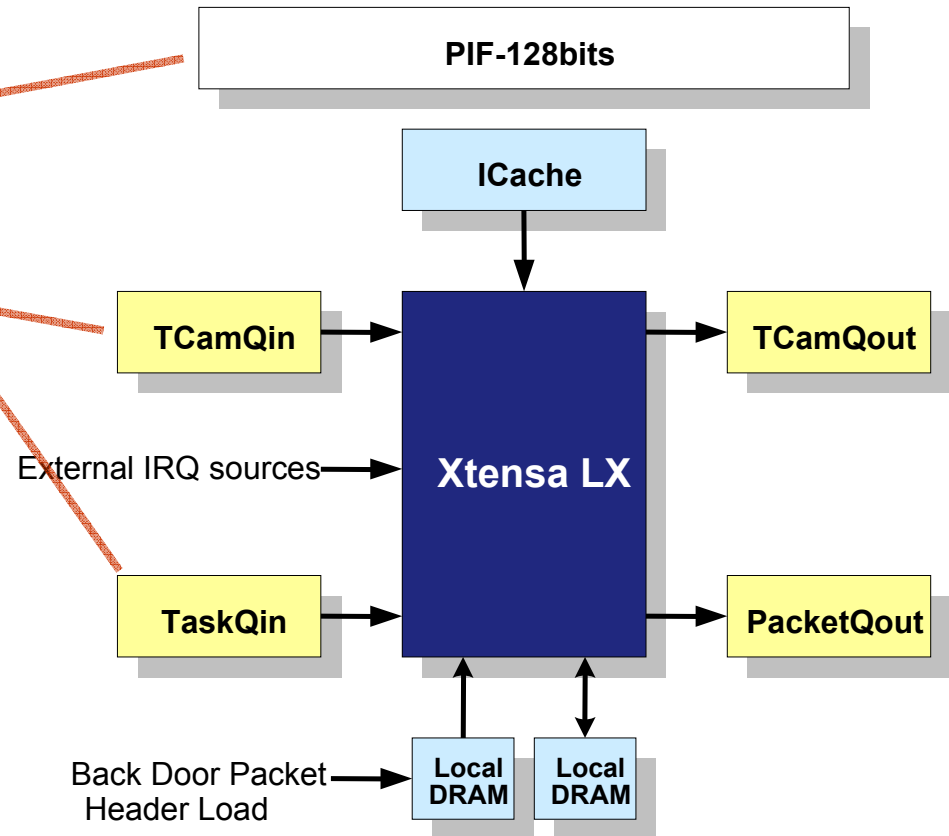
- VLIW Xtensa configuration
- Instructions to accelerate packet processing
- Rich I/O interfaces for high throughput
- Use TCam for lookup

128-bit system interface for high system I/O throughput



128-bit system interface for high system I/O throughput

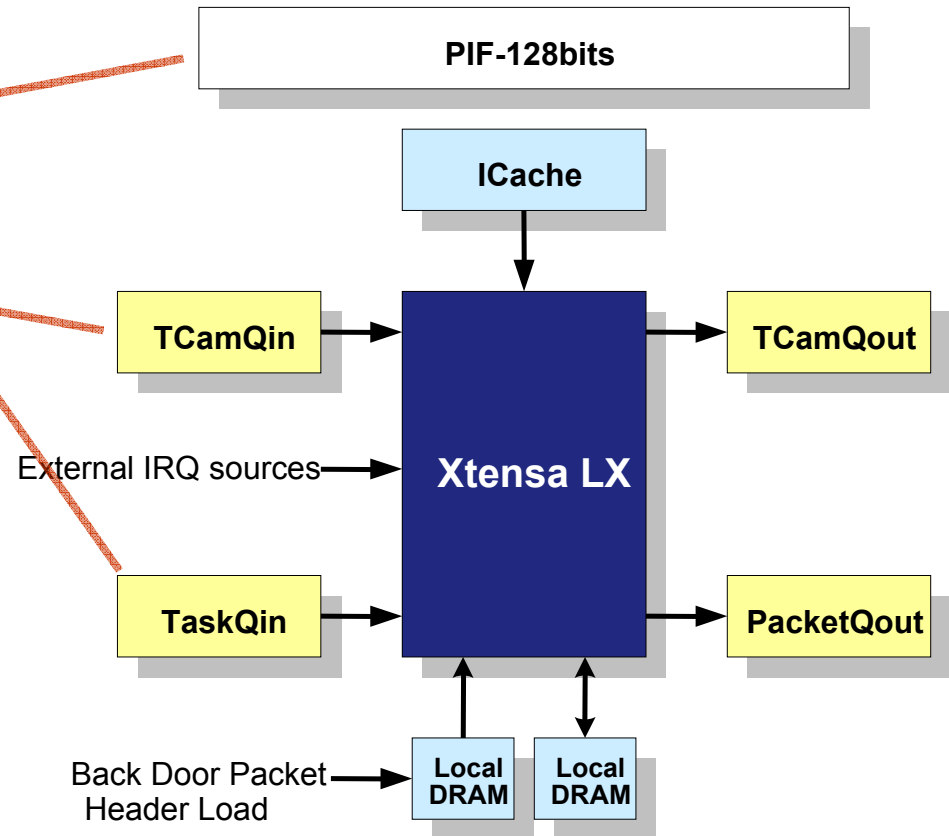
4 TIE Queue (FIFO) interfaces for packet streaming



128-bit system interface for high system I/O throughput

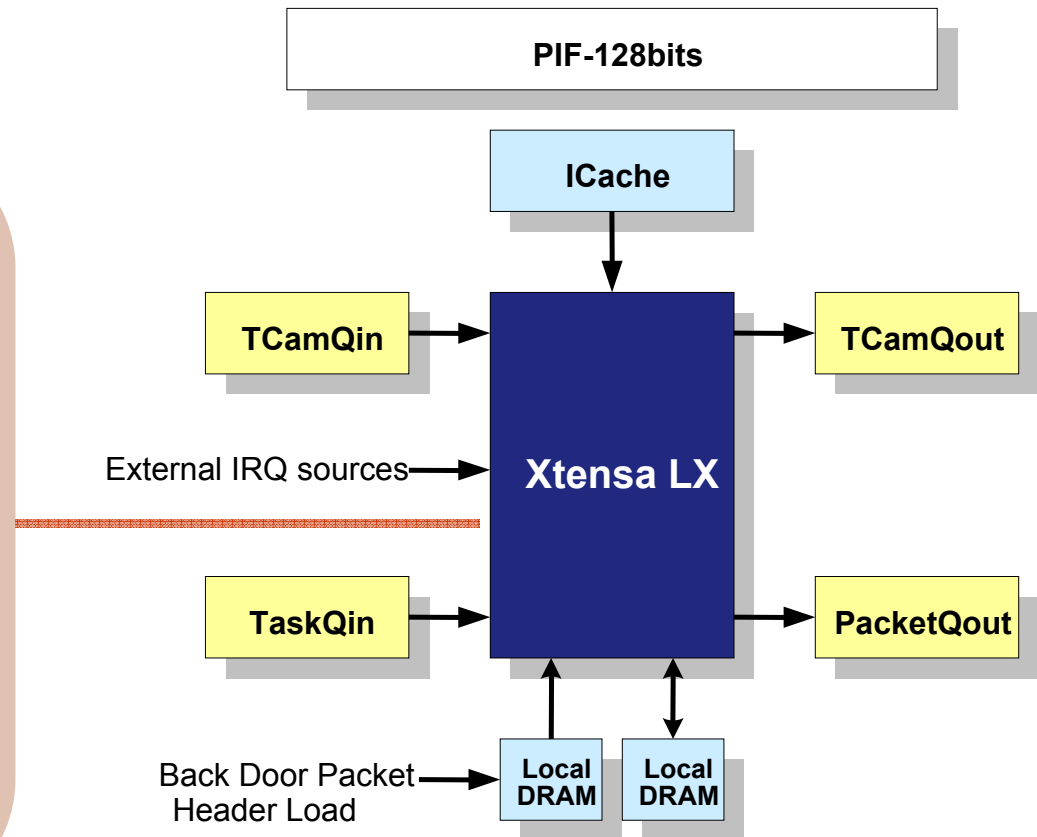
4 TIE Queue (FIFO) interfaces for packet streaming

2 tightly coupled data RAMs for packet headers



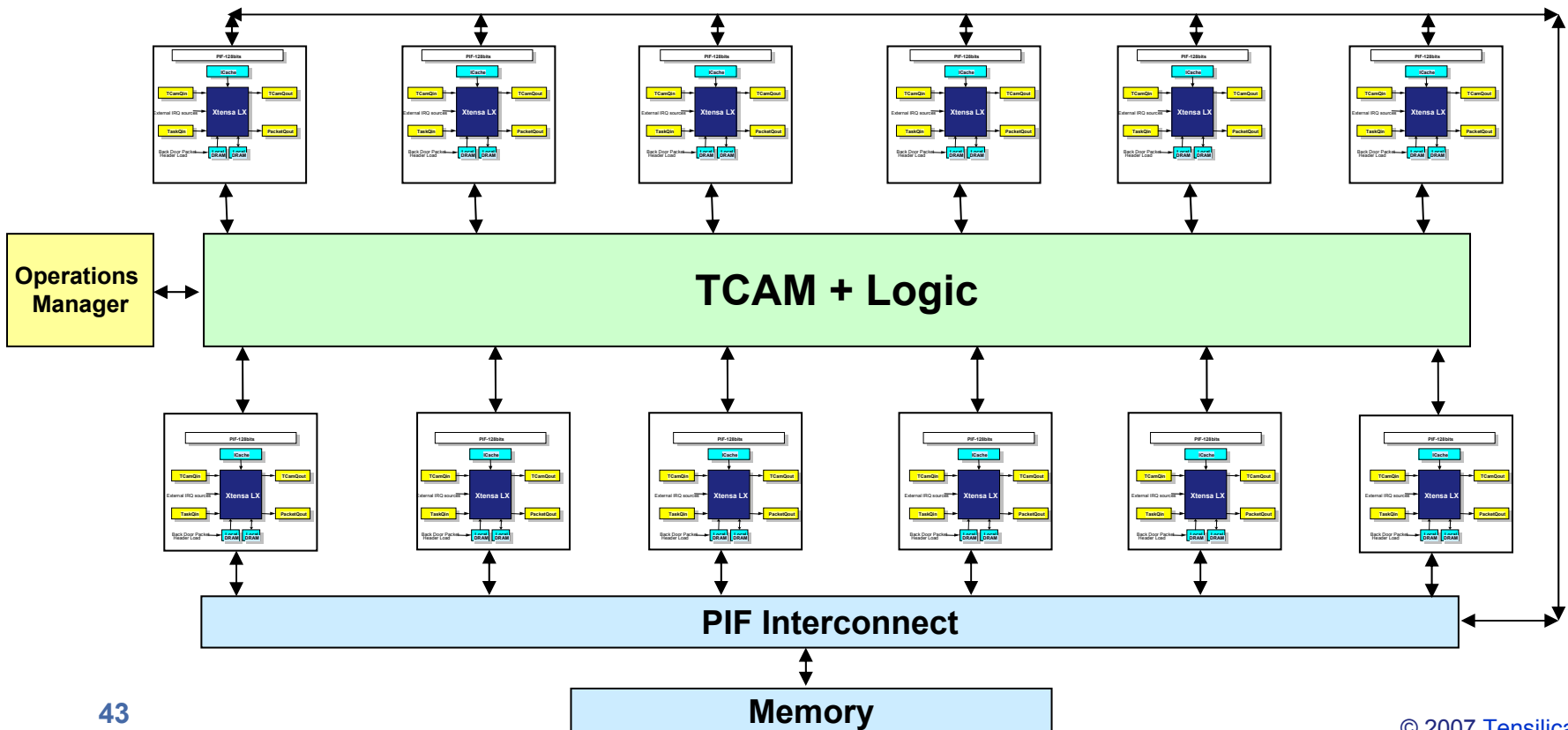
TIE Extensions

- VLIW architecture
- Parse packet header
 - Determine packet type
- Classify packet
 - Based on header field
- Rewrite header
 - Output to downstream engine

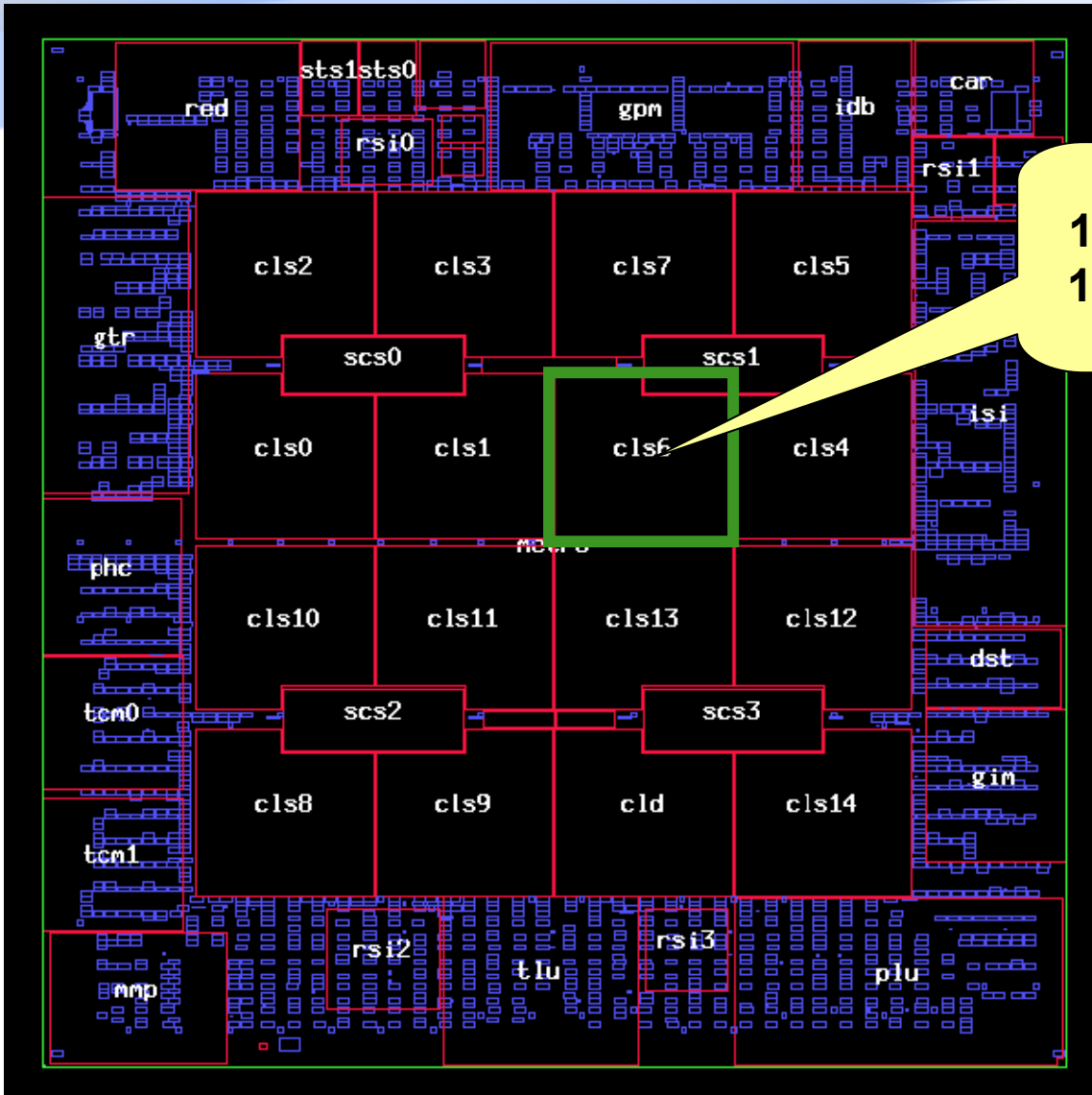


Xtensa for Packet Classification

- For 20 Gbps rate, 12 processor subsystems are required
 - 21 mm² in 90nm technology; 400 MHz



Example: Silicon Packet Processor (SPP) Chip in Cisco's CRS-1



16 clusters of 12 PPEs each

- 188 Xtensa cores on each SPP chip
- 2 SPP chips per linecard
- 96 Gbps bandwidth

Will Eatherton (2005)

Tensilica's Networking & Communications Customers

Networking and Communications



Broad Range of Customer Base

Networking and Communications



Other Industries





Xtensa: High Performance Data Plane Processing

- **Tensilica technology proven for networking and communication applications**
 - Products shipping in volume
- **Xtensa technology addresses NPU needs:**
 - Programmability
 - High data throughput using GPIO and FIFO interfaces
 - Customized to networking for high performance
- **High performance, low energy**
- **Very easy to use with complete toolset**

Find Out More

Visit www.tensilica.com