



The Engines of SOC Design

Diamond 388VDO Dual Core Video Decoder/Encoder

Dennis Moolenaar

Member of the Technical Staff

- **Video encode & decode up to**
 - 720 x 480 @30 fps (NTSC)
 - 720 x 576 @25 fps (PAL)

- **Support multiple coding standards @ main profile**
 - H.264 main profile @ L3 decoder
 - MPEG-4 ASP [no GMC] @ L5 decoder
 - MPEG-2 MP @ ML decoder
 - WMV9/VC1 main profile decoder
 - MPEG-4 ASP encoder

- **Programmable solution**

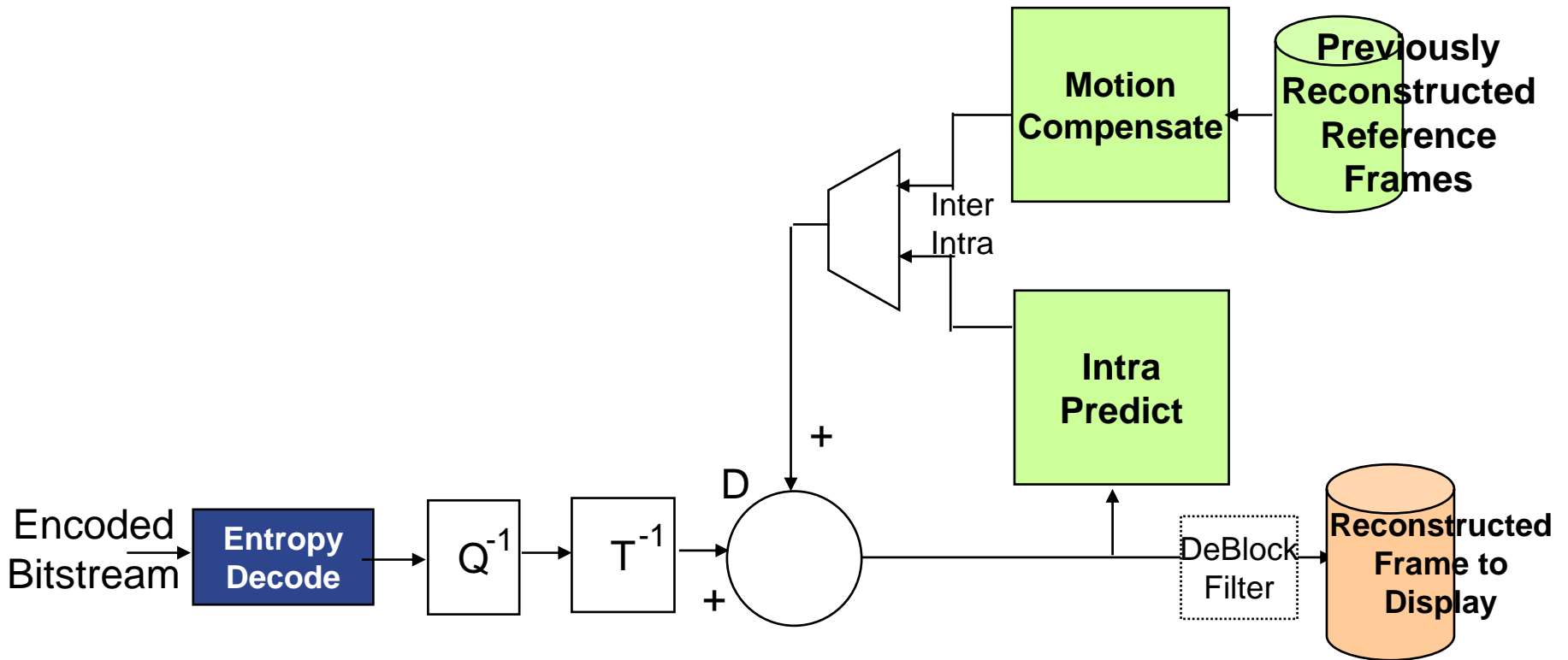
- **Less than 100MB/s memory bandwidth requirement for the decoder**

- **Operating frequency <200Mhz**
 - Can be implemented in 130nm G technology

■ H.264 Main Profile decode cycle requirements on unaugmented Xtensa core

	Million Cycles/sec
Rugby CABAC 5.4Mbps	2518
Rugby CAVLC 5.4Mbps	1918

Video Decoder Data-Flow Path



Two Types of Tasks in Video

▀ Sequential processing

- Decode headers from bitstream
 - Control code
- Decode transform blocks from bitstream
- Decode and compute motion vectors
- Inverse quantization (optional)

▀ SIMD algorithms

- Deblocking
- Motion compensation
- Inverse transform
- Inverse quantization (optional)

■ How many cores?

- Profile the application on the Xtensa cycle-accurate ISS model for a variety of streams (bitrates, complexity)
- Estimate performance gains from ISA extensions for the different algorithms
- => **Two cores minimum (@200Mhz clock frequency)**

■ Homogeneous or heterogeneous?

- Video consists of two types of tasks that need different ISA extensions
- From profiles it was estimated that the cycles on both cores would be balanced
- => **Two heterogeneous cores**

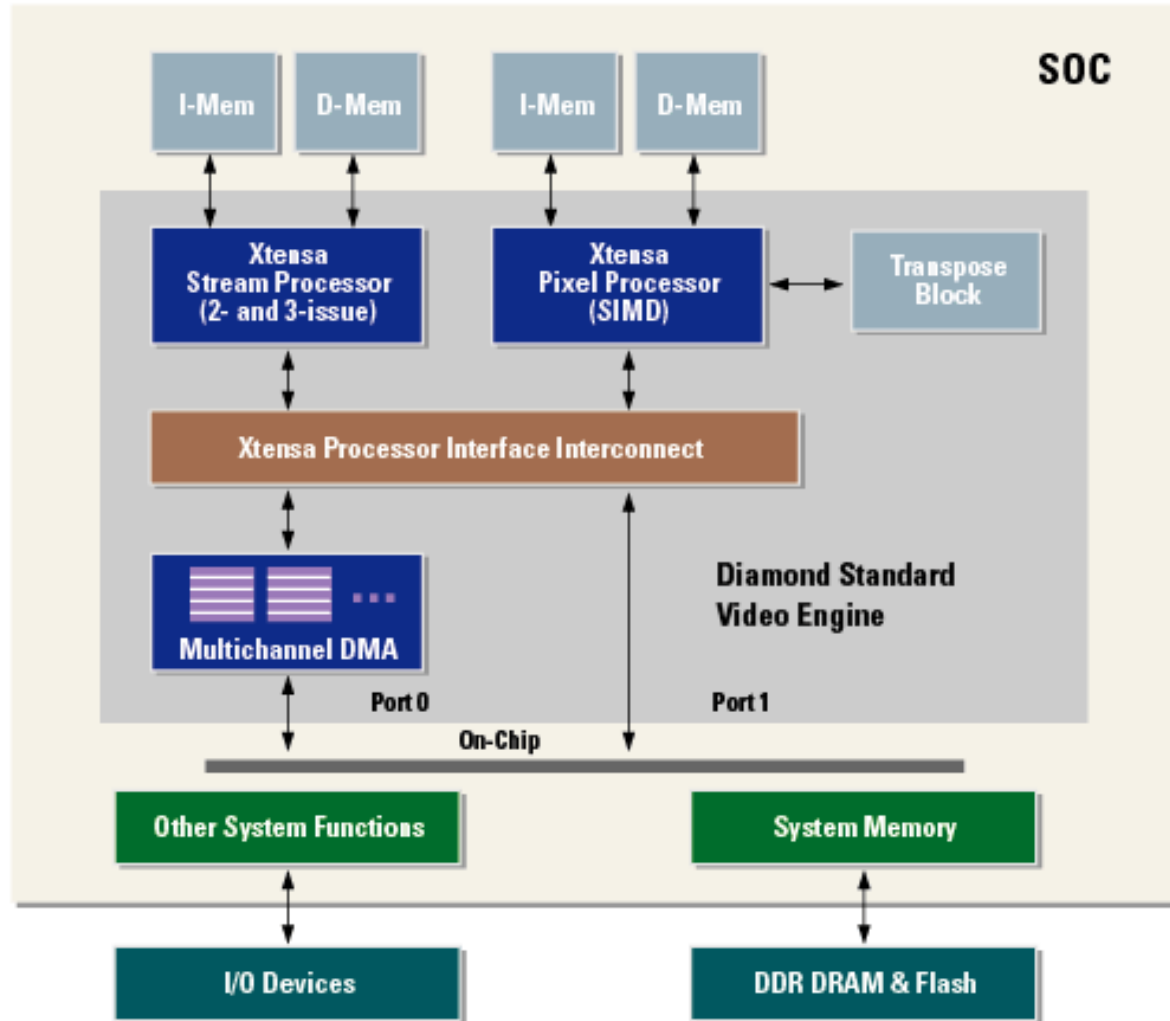
■ **Extend Xtensa ISA**

- Generate instructions as general as possible
 - To support the multiple decode and encode standards
 - To support future codecs
- Use 16- and 8-way SIMD
- Combine basic operations into new instructions
- Design new instructions using high-level Tensilica Instruction Extensions (TIE) descriptions

■ **Design intelligent multi-channel DMA engine**

- Hide external memory latency
- Support DMA from external memory to a core and from core to core (instruction and data memory)

Top Level Block Diagram



■ Stream Processor functions

- entropy decoding, transform block decoding, motion-vector decoding and calculation, control code)
- Set up reference DMAs using decoded motion vectors

■ Pixel Processor functions

- Deblocking, Motion Compensation, Inverse Transform, etc
- DMA reconstructed frames to external memory

Stream Processor configuration

- ISA extensions for sequential function acceleration
 - Fused instructions
 - 2- and 3-issue instructions
- 128b data memory/PIF width
- DMA path to both data/instruction memories

Pixel Processor configuration

- 8 and 16 way SIMD instructions for pixel processing acceleration
- External queue interfaces to transpose block
 - Transpose is a fast row-to-column exchange of an array
- DMA path to both data/instruction memories
- 128b data memory/PIF width

■ Context-adaptive binary arithmetic coding (CABAC) achieves higher compression in H.264

- Our solution: Xtensa ISA extensions
- Peak decode performance is one bin per cycle
- CABAC decoding of one 4x4 transform block:

	Millions of cycles per second
Unaugmented core	710
ISA extended core	13

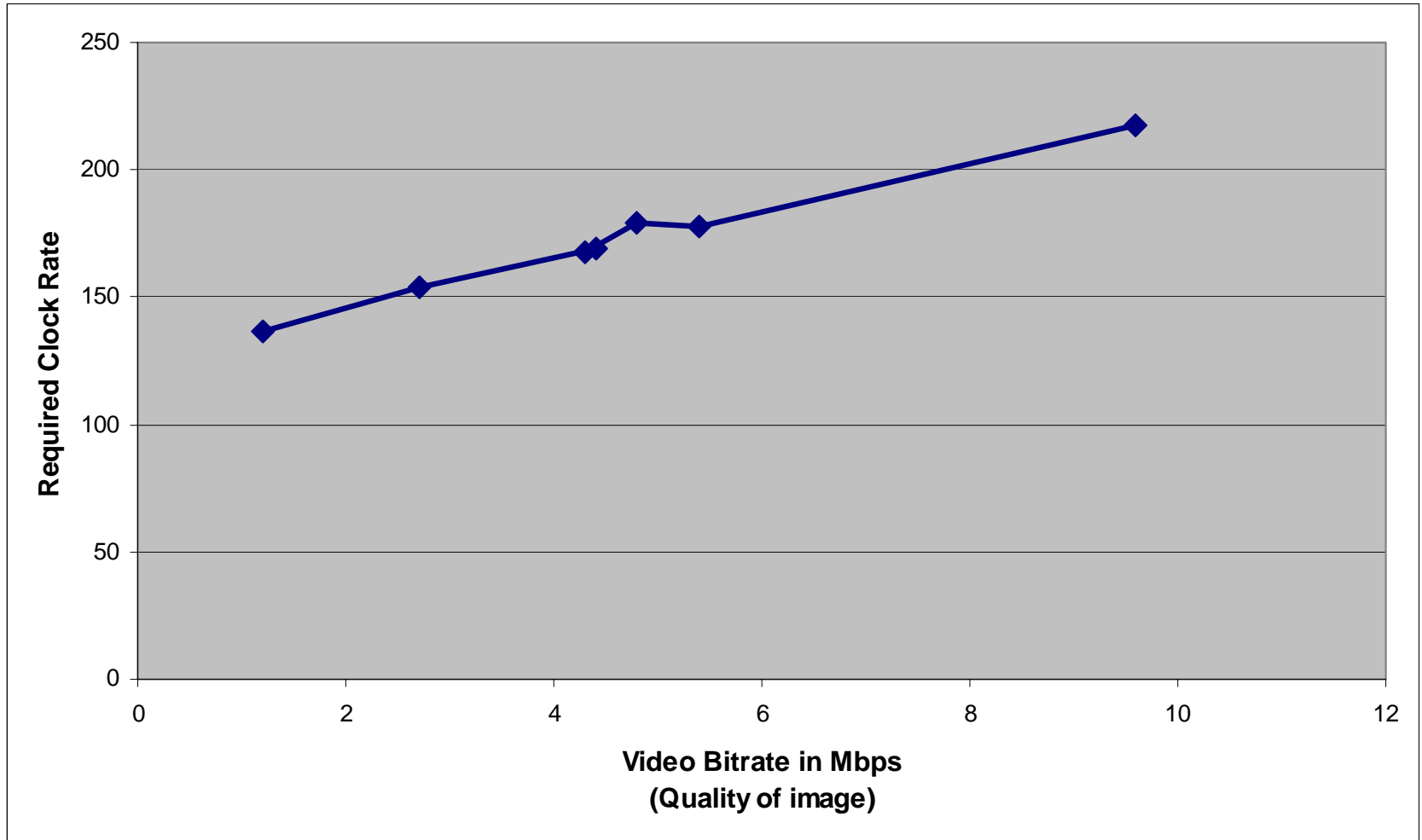
- Area cost: 20K gates for CABAC ISA extensions

ISA Extension Results: Profile Comparison

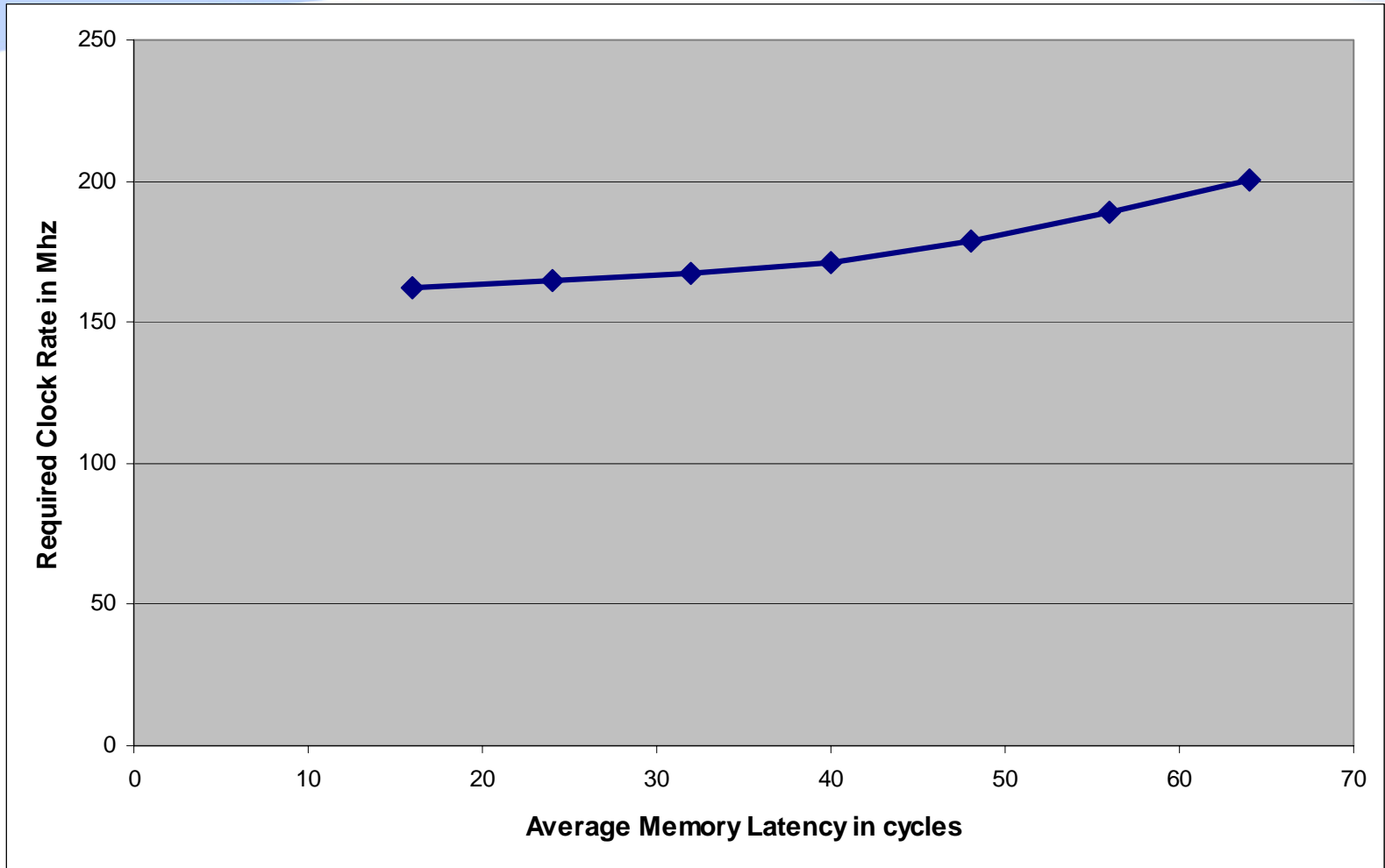
■ H.264 Main Profile decode of 5.4Mbps Rugby stream

	CABAC unaugmented	CABAC ISA extended		CAVLC unaugmented	CAVLC ISA extended
Stream Processor	1,300	174		701	168
Pixel Processor	1,218	178		1,217	162
Total	2,518	352		1,918	330

H.264 Main Profile D1 Decode: Min Clock Rate vs Video Bitrate

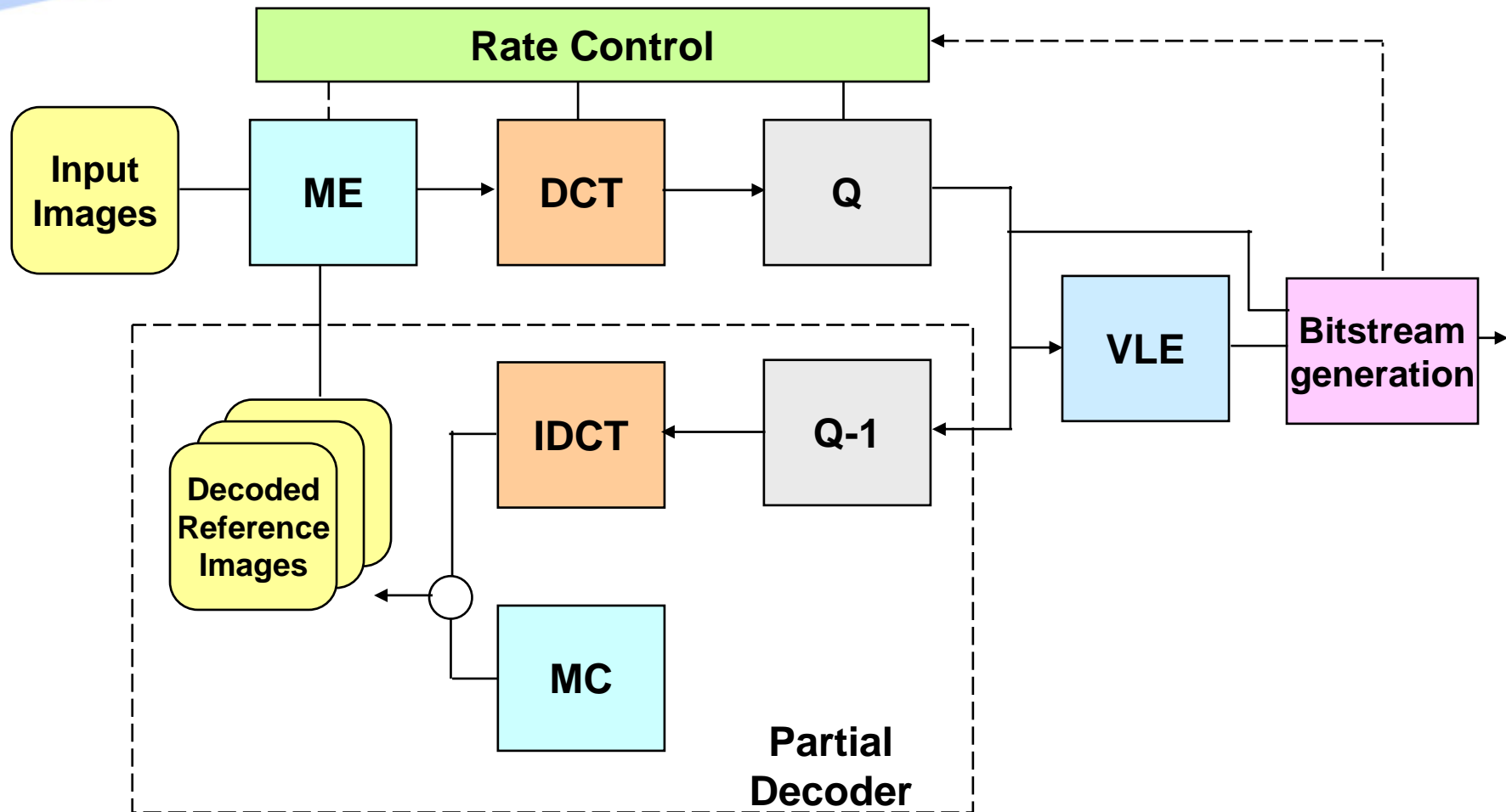


388VDO Can Support Large Memory Latencies



- H.264 Main Profile decode of Mobile Calendar bitstream at 4.3 Mbps

VDO Encoder Block Diagram



■ MPEG-4 performance requirement:

- MPEG-4 Encode requires 4,895 MCPS on unaugmented Xtensa core

■ Most cycles spent in Motion Estimation

	Million of cycles required on unaugmented core
16x16 SAD	527
Diamond	735
Half Pel	1143
8pt SAD	1659
Control	204
Total	4268

Design goal:

Map 4.2 billion cycles into 120 million

Approach:

- **16 way SIMD for fast Sum of Absolute Difference (SAD) calculation**
- **Algorithm optimizations to remove unnecessary loading of data**
- **3 operations per cycle (3-way FLIX)**
- **Optimize control flow with data flow**

Features of Motion Estimation ISA Extensions

- **Fast, flexible and fully programmable**
 - Optimized with generalized Motion Estimation instructions
 - Not specific just to current MPEG-4 encoder implementation

- **ISA extensions support:**
 - 16x16 pixel SAD calculation in 60 cycles
 - Calculates up to four neighboring 16x16 SADs in 100 cycles
 - Four 8x8 pixel SAD calculations in 60 cycles
 - Progressive and interlace support
 - Find best half pel around full pel in 300 cycles (8 SAD calculations on half pel grid)

Motion Estimation Optimization Results

	Millions of cycles required on unaugmented core	Millions of cycles required on ISA extended core
16x16 SAD	527	16.3
Diamond	735	8.4
Half Pel	1143	10.7
8pt SAD	1659	14.2
Motion Estimation	4268	76.2

Area:

Less than 40K gates for all Motion Estimation extensions

■ Cycle requirement: 188Mcycles/sec

- 4.8Bcycles/sec reduced to 376Mcycles/sec

■ Quality comparison between 388VDO and Momusys Reference encoder

	Encoding PSNR difference (dB)
Max degradation	0.205
Max improvement	7.182

- Results of encoding public available VQEG YUV sequences

■ Encoder bandwidth requirement 148MB/sec

Diamond 388VDO Performance

	Standard	Resolution	Frames per sec	Bit Rate	DDR Memory Bandwidth	Required clock rate
Decode	H.264 Main Profile Decode	D1	30	5 Mbps	86.3 MB/s	162 MHz
	VC-1/WMV9 Main Profile Decode	D1	30	6 Mbps	88.9 MB/s	172 MHz
	MPEG-4 Advanced Simple Profile Decode	D1	30	6 Mbps	59.8 MB/s	167 MHz
	MPEG-2 Main Profile Decode	D1	30	8 Mbps	46.1MB/s	151 Mhz
Encode	MPEG-4 Advanced Simple Profile Encode	D1	30	4 Mbps	148 MB/s	188 Mhz

- Bit Stream: Mobile Calendar
- Memory Latency = 32

■ Flexibility

- Full software programmability allows easy adaptation to rapidly evolving video standards and solutions

■ Low cost

- Hits performance goals in mature, low-cost 130nm G process
- Small footprint (size < 11mm² in 130nm G)

■ Low clock rate (< 200MHz)

■ Low external H.264 decoder memory bandwidth requirement (< 90MB/s)

■ Available: NOW