The Configurable Processor Company

Throttle IP Core Power Dissipation:

Use RTL Power Analysis Early and Often

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Problem Statement

- **SOC power dissipation is growing due to increased number of transistors**
  - Power dissipation is an important design goal and is no longer a design byproduct that you get as a result of achieving functionality and speed goals
- **Use of multiple microprocessor cores on an SOC is growing**
  - Processor core power dissipation is an increasingly important factor in SOC power dissipation

These trends encourage the use of early power analysis to meet SOC design goals

Gate-level power simulation increasingly less effective because:

- **Gate-level netlists not available until late in the design**
  - Too late to make design changes
- **Gate-level netlists flatten design hierarchy, making power analysis down to the module level difficult**
- **Growth in transistor count**
  - Simulation times too long to be performed continually
  - You tend not to run as many gate-level simulations as before

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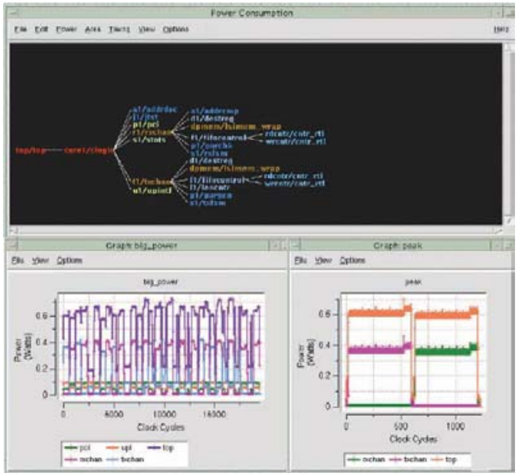
Solution: RTL power analysis

- **RTL test bench is generally up and running early in the design cycle**
- **RTL power-analysis reports preserve design hierarchy**
  - Makes it easy to identify power-saving opportunities at the module and even the leaf-cell levels
- **Runs faster than gate-level power simulations**
- **We used Sequence Design's PowerTheater for RTL power analysis**

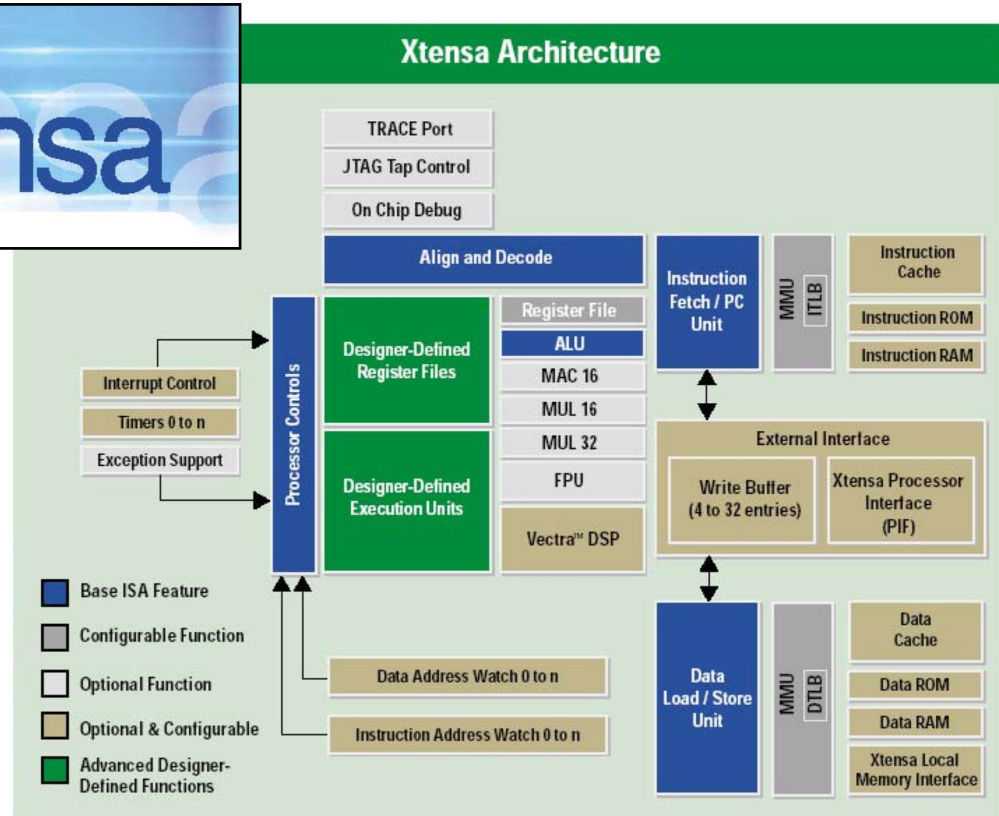


PowerTheater

Test case: Xtensa configurable processor

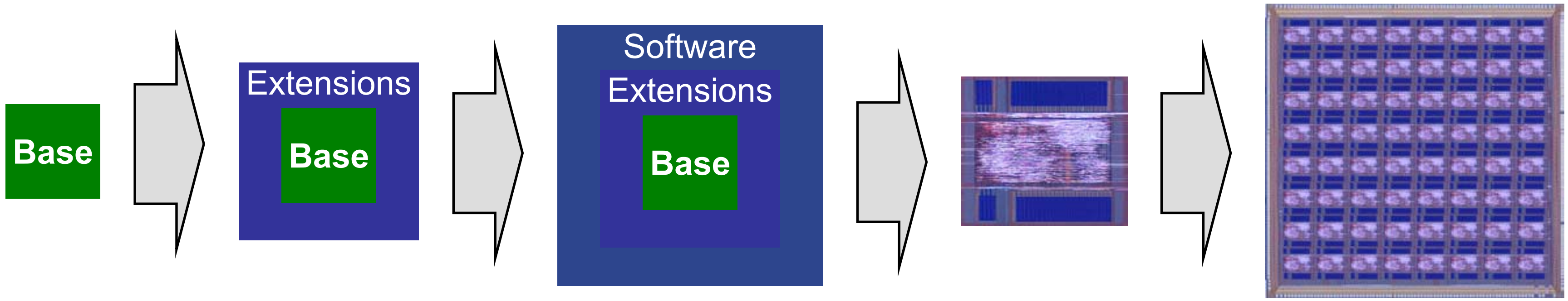
New Xtensa microprocessor design

Design goal: reduce power dissipation by 25%



A configurable processor primer

- **Low Cost**
  1. start with tiny core
- **High Performance**
  2. extend to fit application
- **Design Productivity**
  3. automate software and RTL generation
  4. automate hardware generation
- **Sea of Processors**
  5. use as basic building block to create programmable SOCs

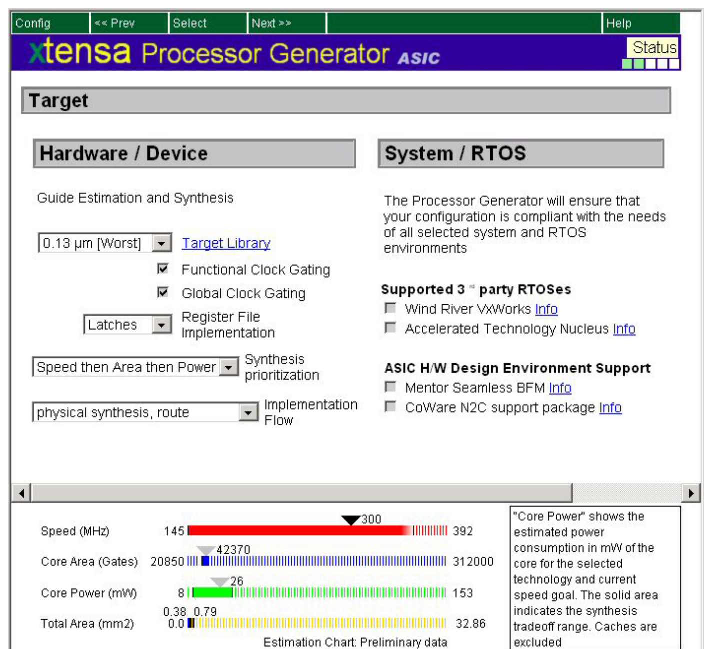


1. 2. 3. 4. 5.

Special challenges for configurable IP cores

- Configurable cores have numerous combinations to test
- Soft IP must be characterized for various fabrication processes
- Requires a database of area, timing, and power numbers for real-time estimation

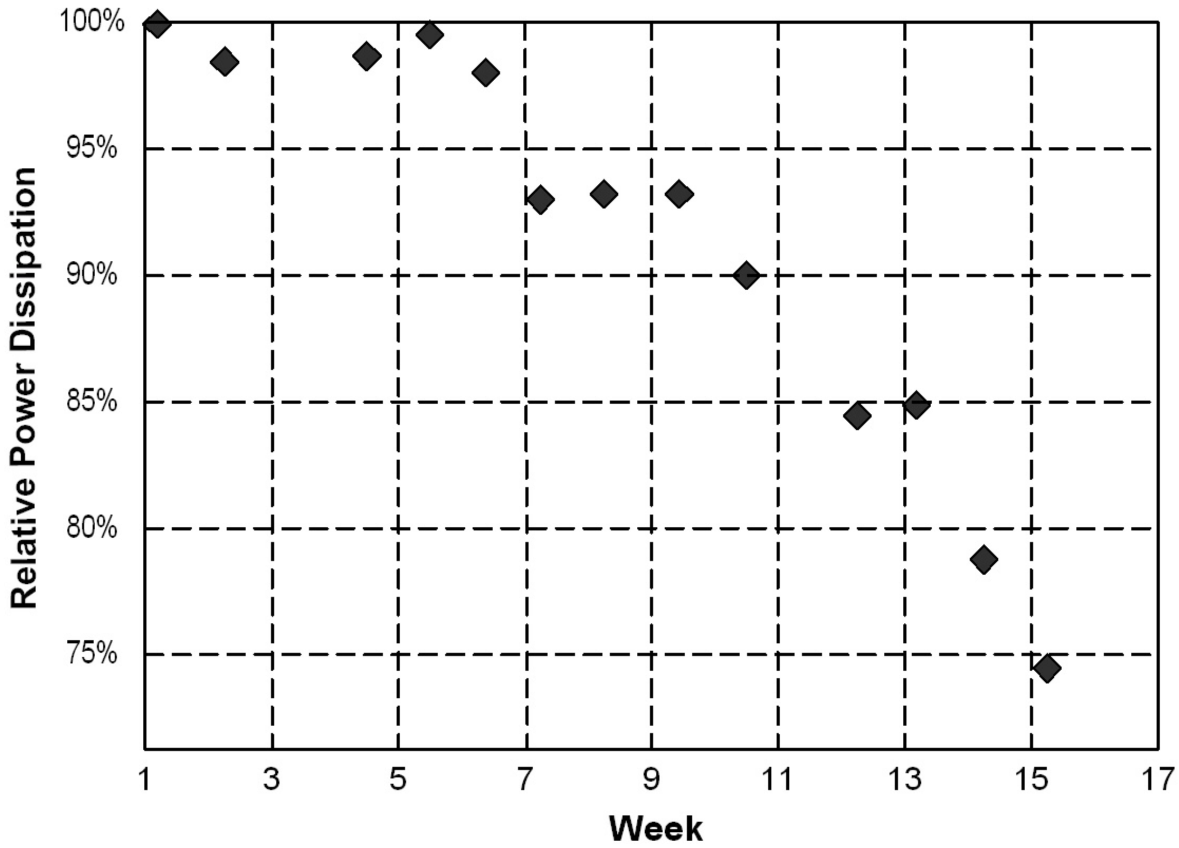
Real-time speed, power, and area estimation



Power-analysis test method

- **Run weekly power regressions as soon as RTL test environment is operational**
- **Detailed power-analysis results posted on company intranet**
  — Team members get ready access to power-analysis results
  — Reports give hierarchical breakdown by module and sub-module
- **Results of power-reduction efforts appear as soon as next week's report**
- **Plot weekly results to show progress towards goal**

Weekly plot



Goal met: 25% power reduction in 15 weeks.

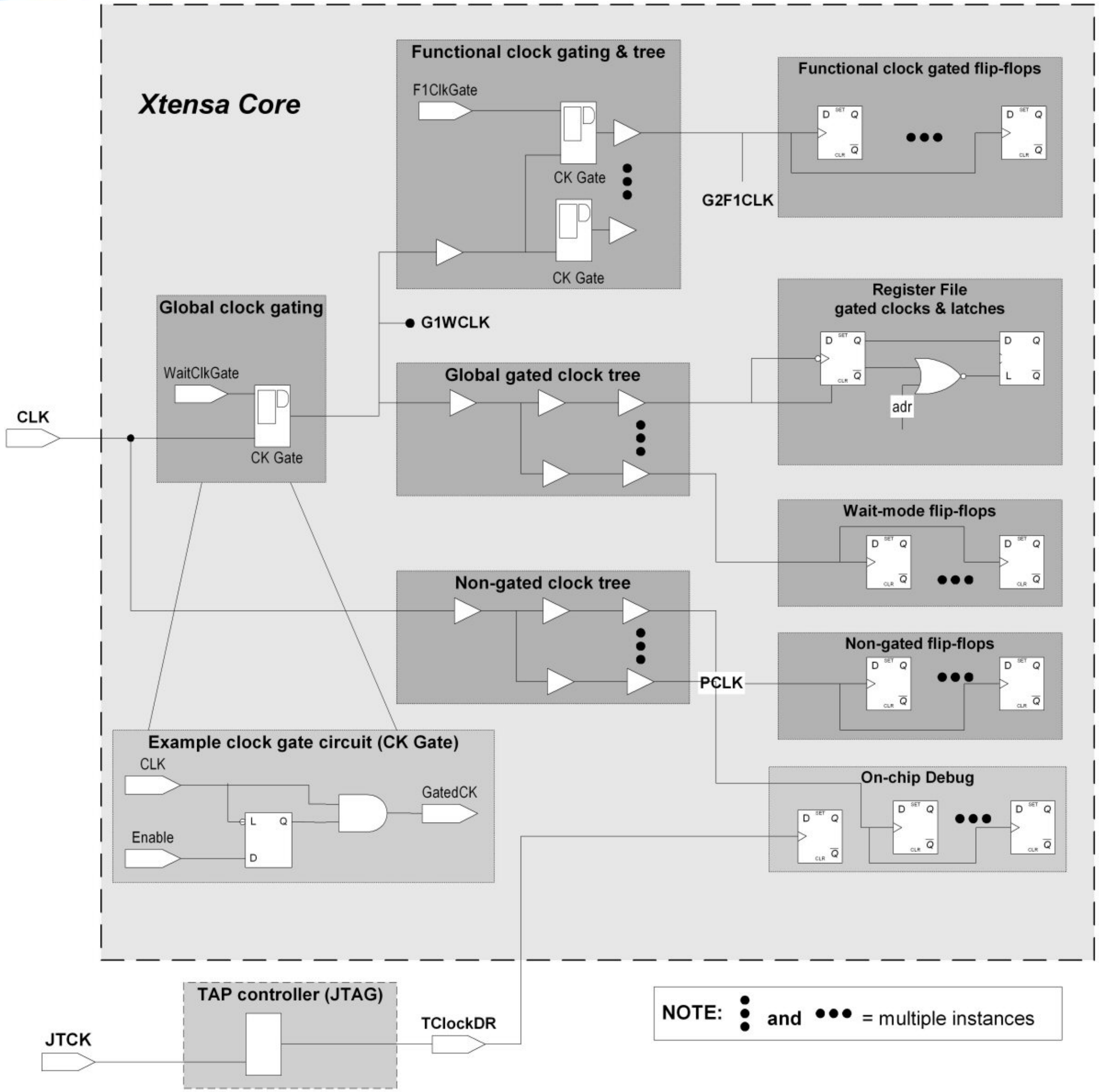
Benefits of the weekly graph

- **Any design change that spikes power is quickly spotted**
  - — Module responsible for the spike is quickly identified
  - — Remedial action can be performed quickly and on the right module
- **Quantitative record**
  - — Proves the effectiveness of power-reduction efforts

Clock gating and the Xtensa processor

- **Clock gating is a common technique used for reducing dynamic power**
- **Xtensa processors employ two types of clock gating**
  - Global
  - Functional
- **Used RTL power analysis to measure the effectiveness of clock gating in our design**

Clock gating in the Xtensa processor



Power-analysis test evolution

1. **Use existing verification tests**
2. **Develop specific regression tests for power analysis**
   — Sleep-mode test
     Test global clock gating
   — NOP test
     Initial functional clock-gating test
   — Module-specific tests (example: DSP)

Sleep-mode test

- **Global clock gating active when processor is in sleep mode**
  - — Any modules dissipating dynamic power should do so for a reason
- **OCD module had surprisingly large power dissipation**
  - — Additional clock-gating opportunities identified in the OCD module
  - — OCD sleep-mode power dissipation reduced by 50%
- **OCD module was not a big user of power**
  - — It's power dissipation characteristics were previously ignored because they were small
  - — RTL pinpointed the OCD module's power dissipation as an easy target for power reduction
- **Cut the power dissipation of enough modules by 50% and you get substantial power savings**

NOP test

- **Processor runs nothing but NOP instructions**
  - Exercises instruction-fetch and –decode modules
  - Most other processor modules should be inactive
- **Sets a lower bound for processor’s active power**
- **First-level test of functional clock gating**
- **Identified legacy power creep**

Legacy power creep

- **NOP test identified a leaf cell that didn’t use clock gating, but should**
- **Cell was originally designed for a few narrow registers**
  - Didn’t use clock gating to save gates
- **Cell was eventually used by several other designers in other modules**
- **Adding clock gating to this one primitive significantly reduced NOP-test power dissipation**

Module-specific power-analysis tests

- Exercise a module's logic as much as possible
- Example: FIR kernel assembly code tests processor's DSP extensions
- Regression testing of DSP extensions later caught a power inefficiency that was introduced by a design change made towards the end of the design phase

Conclusion

To meet aggressive power budgets for IP, designers must focus on power consumption throughout the design phases

- Start RTL-level power analysis early in the design
- Regularly run power-analysis regressions
- Monitor the effects of design “fixes” on power dissipation