



The Engine of SOC Design

## Energy Breakthrough in Chip Design

*Big Challenges, Bigger Rewards*

Chris Rowen – Globalpress Summit  
March 2008



## Agenda

- Moore's Law, Power and the Environment
- Processors and Multi-Core
- The Formula for Success
- Rethinking the Cores
- Rethinking Multi-core
- Innovation Examples
- Global Impact





# Electronics Inefficiency is a Global Problem

Direct energy use for all Information Technology (PCs, telephony, consumer electronics, corporate)

6% of all electricity

200,000,000,000,000 watt-hours per year  
(~30 800MW central baseload power plants) for U.S. alone

Nearly 150 million tons of CO<sub>2</sub> per year

Equivalent to 30 million cars

Lack of smart energy management in other major energy uses:

Cars

Lighting

Heating

Needed: more energy efficient designs



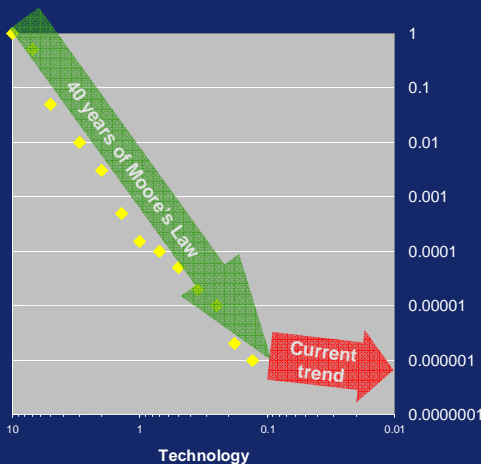
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# Moore's Law No Longer Helps Power

Silicon Energy Efficiency



*The only good answer is parallel functions*

1 block:

Frequency	1
Voltage	1
Power	1
Area	1
Throughput	1



2 blocks in parallel:

Frequency	0.5
Voltage	0.5
Power	0.25
Area	2
Throughput	1



Tensilica cores have been characterized to 0.6v

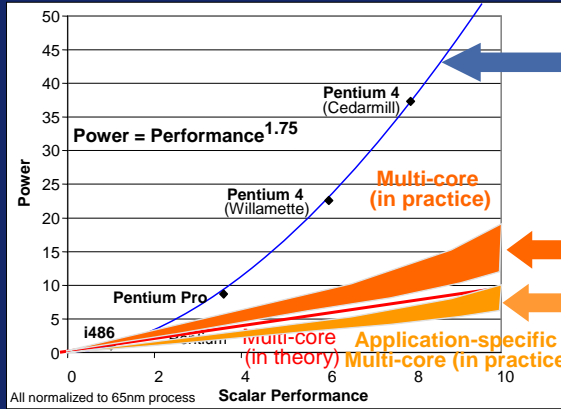
Source: Shekhar Borkar, Intel, "Exponential Challenges, Exponential Rewards—The Future of Moore's Law", 2004

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# Multi-Core Processors Lower Power



Single Core = Exponentially More Power for Performance

Multiple Small Cores = Performance at Much Lower Power

Application-specific processor tuning further improves performance and reduces energy

Source: John Paul Shen, Intel Microarchitecture Research Lab  
WCED Panel: June 18, 2006

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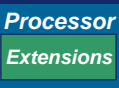
# Low Energy Processor Breakthrough 1 optimized instruction = 5-50 RISC instructions



Select or describe processor configuration



Xtensa Processor Generator

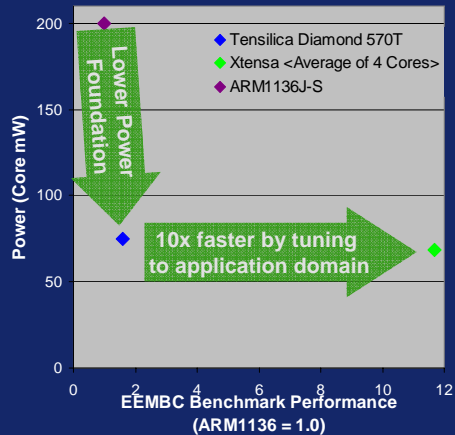


Complete Hardware Design



Complete Software Environment

Power and Performance (130nm)



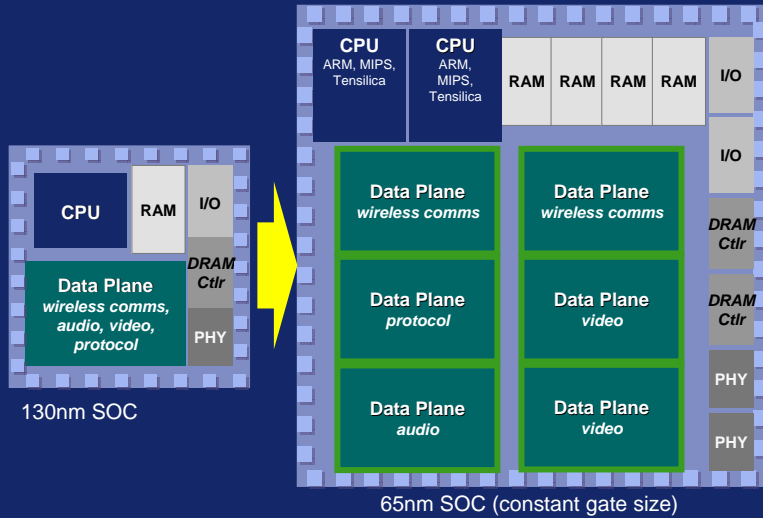
Performance on EEMBC benchmarks aggregate for Consumer, Telecom, Office, Network, based on ARM1136-J-S (Freescale iMX31), Tensilica Diamond 570T, Xtensa LX, T1050 and T1030. All power figures from vendor websites, 2/23/2006

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## Number of Processors Increasing with Smaller Geometries



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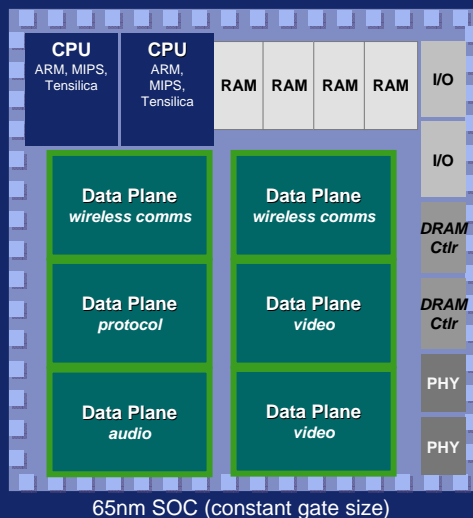
## Control and Data Plane Opportunities for Processors

### Control Plane:

- New more performance
- Need general-purpose CPUs
- Big challenge: Rewriting software for parallel execution
- Hard to use multiple cores

### Data Plane:

- Need **lots** more performance
- Shift underway to processor-based data-plane
- Parallelism among functions is obvious – easy to use multiple cores
- Big challenge: Finding common architectures to ease integration



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# Formula for Energy Efficiency Success

## Multi-core Design

- Many small cores
- Interfaces, memory and bus
- Modeling and software development

## + Optimized Processor

- Easy to modify for exact application and lowest power
- XPRES Compiler: automatic processor generation
- Mobile Audio/Video DSP solutions
- Low-power Linux processors

## = Energy Breakthrough

- Battery life and mobility
- Simplified packaging, power, cooling
- Reduced product and operating costs
- Lower environmental impact

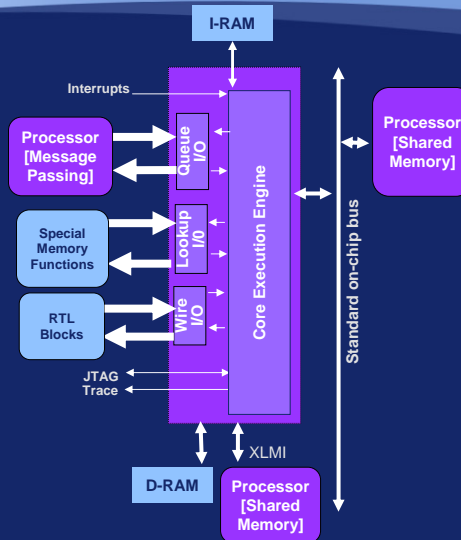


# Multi-Core Demands New Communications Support

Conventional processors have limited communications potential

Xtensa creates a huge range of memory-mapped and direct connection options

- Shared memory communication interfaces
  - on system bus
  - in local memory
- Message-based communication interfaces
  - Direct connect input/output wires
  - Input and output queues
  - Lookup interfaces create any number of memory ports
- Cuts communication overhead
  - No load or store instructions required to directly access data
  - Synchronization is built-in





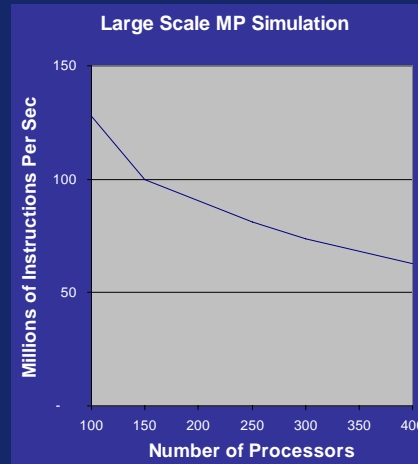
## Required for Multi-Core Design: Modeling and Simulation Tools

Advanced chip design needs multi-core tools

- Architectural exploration
- Modeling and analysis
- SW development and debug

Example: Modeling

- ARM RealView SOC Designer
- VaST Virtual System Prototypes
- CoWare ConvergenSC
- Mentor Seamless
- Tensilica XTMP and XTSC



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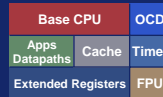
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## Optimize Processor for Power: Xenergy Energy Explorer

New GUI

Processor Description



Application Code

```
int main( ) {  
  int i;  
  short c[100];  
  for ( i=0; i<N/2; i++)  
  {
```



Tune processor  
instruction set  
and memories

Tune software  
algorithms and  
coding

Function Name	Total energy (%)	Function energ...	Cumulative ene...
__start	99.45	46399165	46653523
_ResetHandler	0.34	161403	25458
__call_extprocs	0.04	21168	92955
__do_global_dtors_aux	0.02	12852	71787
__do_global_ctors_aux	0.02	11192	58935
__atexit	0.01	7821	47743
__library_init	0.01	6751	39922
__exit	0.01	5808	33171

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## Xenergy Proves: Energy Improvements up to 83x

Configuration		Dot Product	AES	Viterbi	FFT
Base Xtensa	K Cycles	12	283	280	326
	Energy ( $\mu$ J)	3.3	61.1	65.7	56.6
Optimized Xtensa	K Cycles	5.9	2.8	7.6	13.8
	Energy ( $\mu$ J)	1.6	0.7	2.0	2.5
Energy Improvement		<b>2x</b>	<b>82x</b>	<b>33x</b>	<b>22x</b>

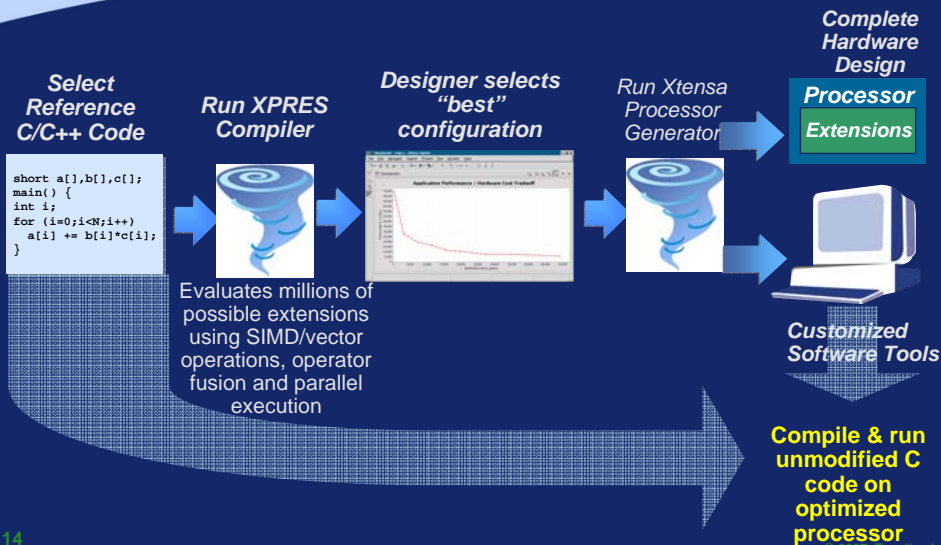
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## Automatic Processor Generation: XPRES Compiler

Great for DSPs



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## Tensilica Delivers Broadest DSP Range

1. General-purpose communications DSP packages, C/C++ compilers, libraries:
  - MAC16 option package [1 MAC]
  - VetraLX option package [4 MAC]
  - Diamond 545CK core [8 MAC]
  - Diamond 570T CPU+DSP core [1 MAC+2x32 MUL]
2. Multimedia DSP packages, C/C++ compiler, full codec packages
  - HiFi2 audio option package, with full audio codecs [2 MAC]
  - Diamond 330HiFi audio core with full audio codecs [2 MAC]
  - Diamond 388VDO video code with full video codecs
3. DSP architecture generator, C/C++ vectorizing compiler support
  - XPRES Compiler for automated DSP design [many MAC]
4. Customer-specified DSPs
  - Specify a wide range of custom DSP architectures for any data-type, operations and performance level [many MAC]
  - Expert architecture help from Tensilica

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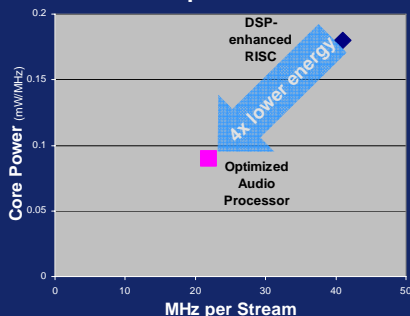


## Data Plane Example: Real World Multimedia Processors



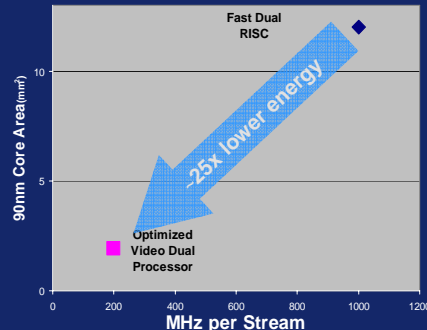
### Audio

#### AACplus v2 decode



### Video

#### H.264 D1 decode



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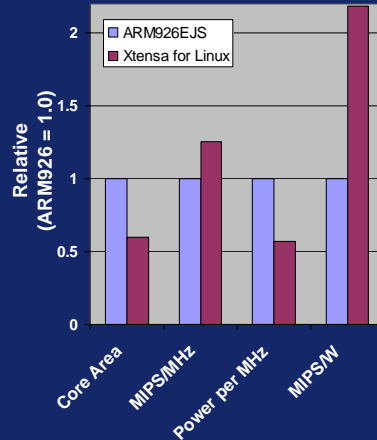
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## Control Plane Example: Low-Power Linux for Mobile



- Linux OS demands:
  - High general-purpose performance
  - Complex memory management features
- Tensilica Xtensa configured for low-power compared to most efficient ARM core for Linux
  - 40% smaller core
  - More than 2x the energy efficiency



90G process technology

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## Example: Cisco's QuantumFlow Processor

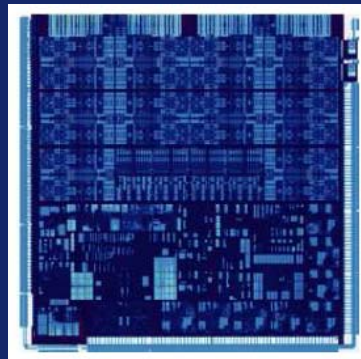


40 Xtensa cores  
4 threads per core  
400mW per core @ 1.2 GHz - 90nm



New Cisco ASR 1000 Family

*The highest performance processor chip for a general-purpose architecture: >50,000 MIPS*



Nikhil Jayaram, director of engineering, Cisco.  
"They [ARM, MIPS, PowerPC and Tensilica] were fairly similar but the Tensilica architecture had some clear benefits when you dip down into the gory details of network processing."  
EETimes, March 3, 2008

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# Example: Consumer Printers

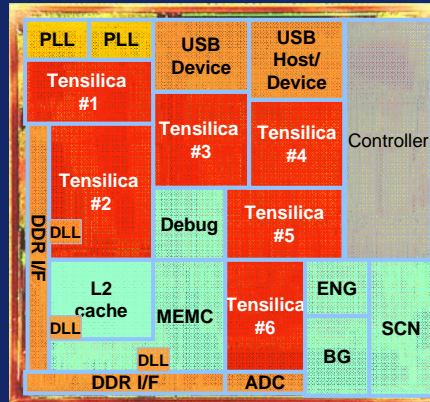


## Most Top Printer Makers Use Tensilica

EPSON's REALOID heterogeneous, asymmetric, 6 Xtensa core design with little hard-wired logic



EPSON PM-D870



Epson REALOID IC Block Layout

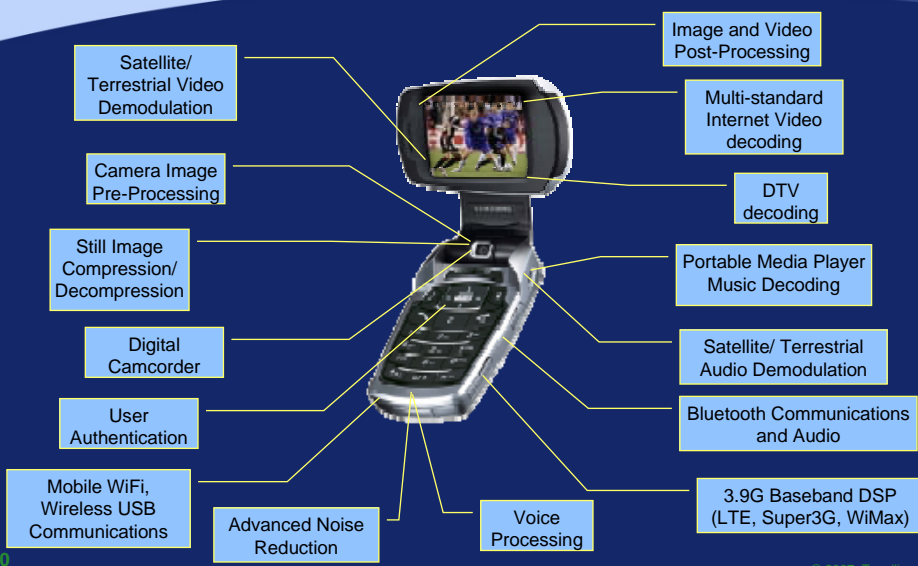
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90nm process technology, 100-200 MHz clock rate, 5-10M gate-count complexity, Less than 2.5W power  
For more details, see the EPSON presentation from the 2006 Nikkei Electronics Processor Symposium / Multi-Core Expo Japan

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# Example: Mobile Feature Integration



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## New Approach: New Opportunities for Innovation

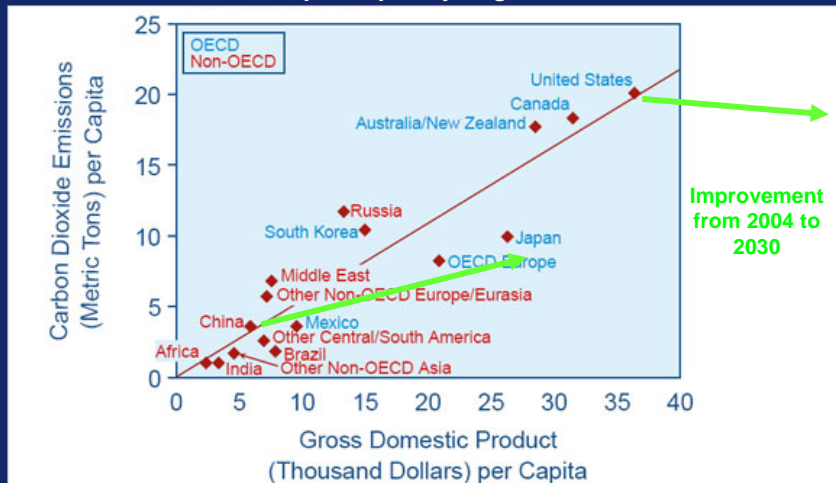
Multi-core Design + Optimized Processor = Energy Breakthrough

Energy Efficiency = New Design Success



## Global Impact: Quality of Life

Carbon Dioxide Emissions and Gross Domestic Product per Capita by Region 2004



Source: Derived from Energy Information Administration, International Energy Annual 2004 (May-July 2006, web site [www.eia.doe.gov/iea](http://www.eia.doe.gov/iea))