



The Configurable Processor Company

IP Forecast

Fundamental Change in IP+EDA Opportunity

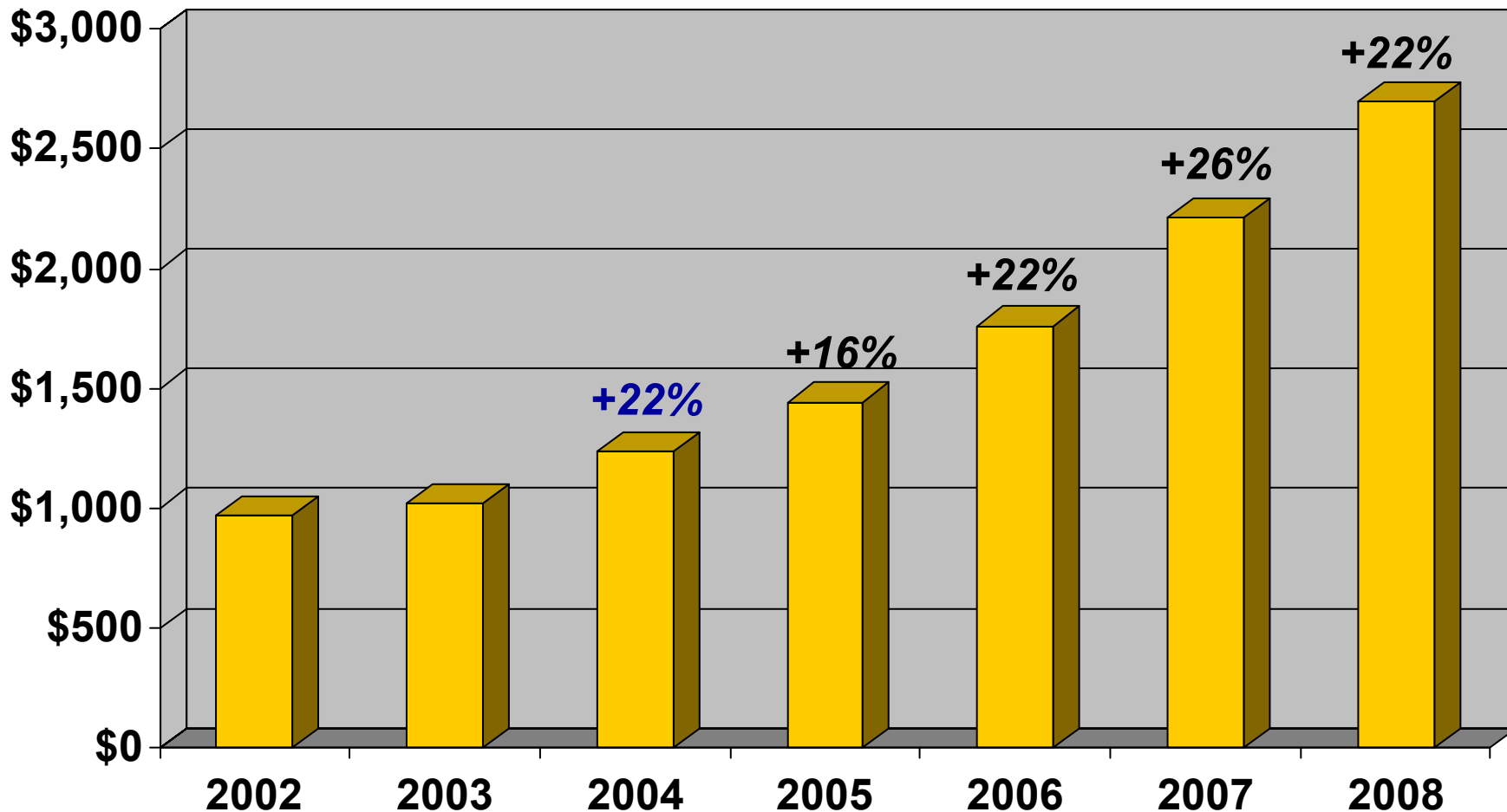
Chris Rowen

President and CEO, Tensilica



IP: A Growing Part of SOC Design

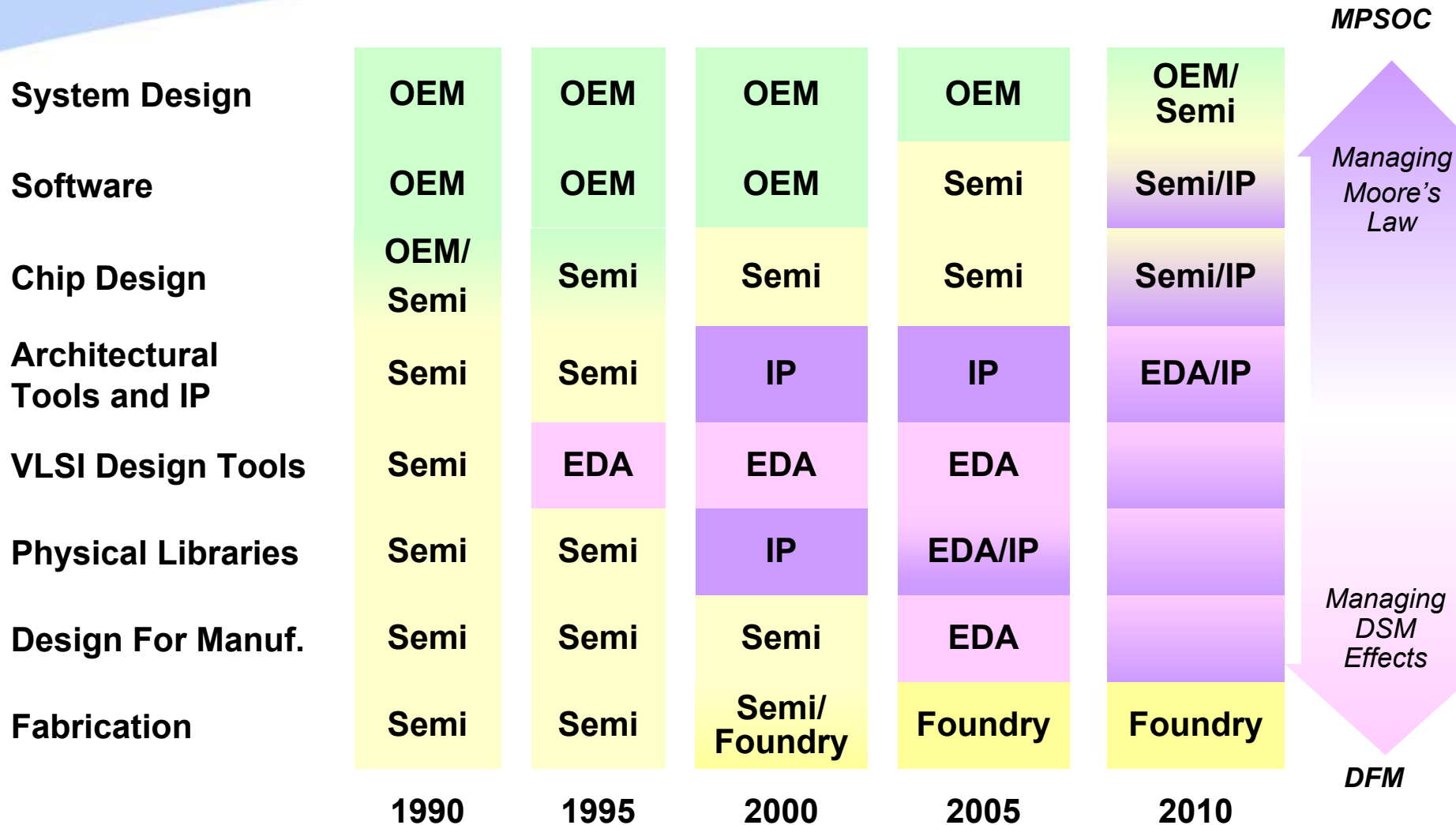
Commercial semiconductor IP revenue (\$M)
+ annual growth%





The Evolving Silicon Food Chain

EDA and IP Merging and Moving Up



tensilica *A Processor and Application-Centric World*

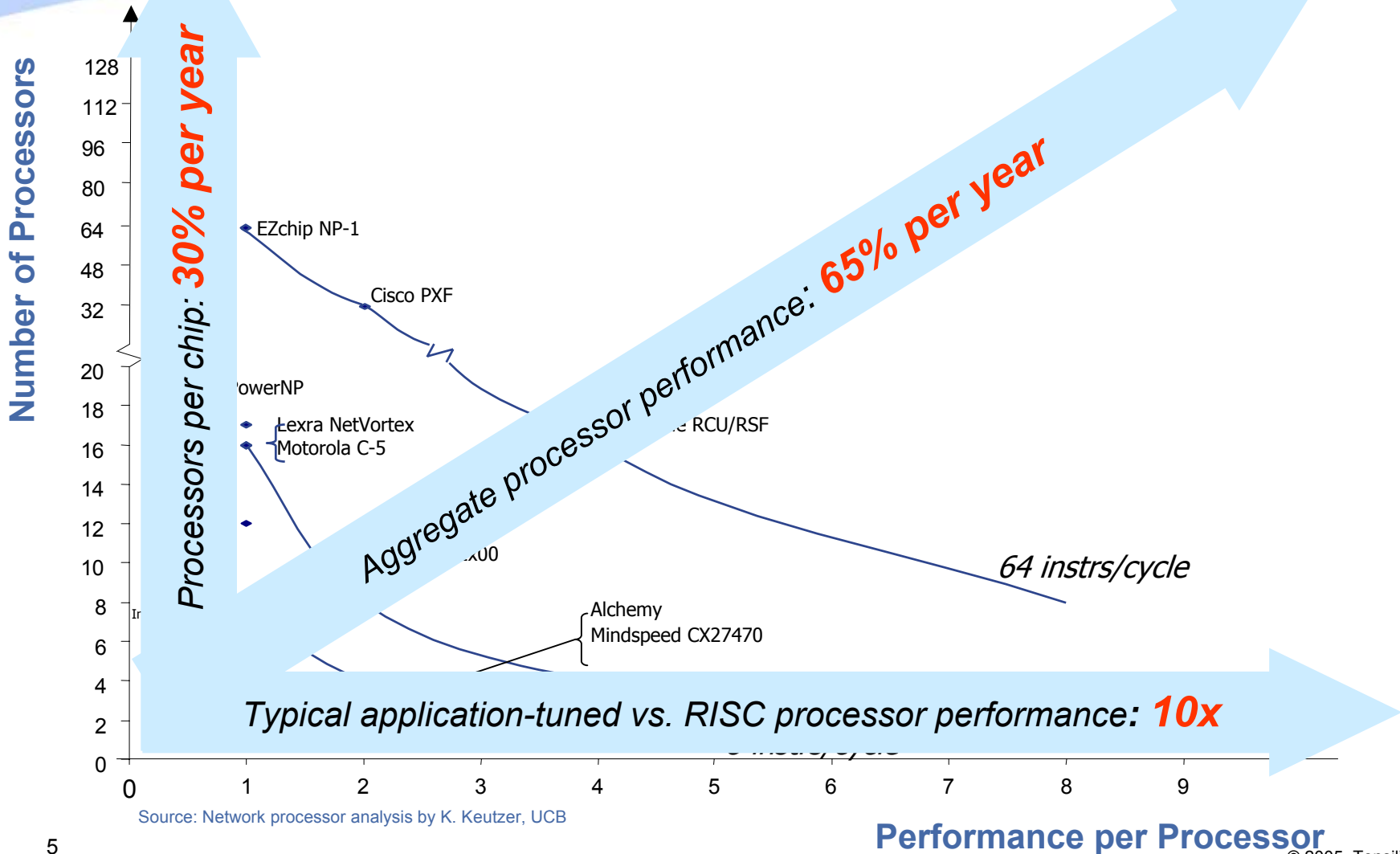
	<i>Hardware</i>		<i>Software</i>	
<i>System Planning</i>	System Specification and Architecture		Algorithm Invention	<i>Application Centric</i>
<i>Partitioning</i>	Communication and Computation		Application Implementation	
<i>Hardware/ Software Integration</i>	Processor to Bus & Memory Organization		SW Integration	<i>Processor Centric</i>
<i>Block Integration</i>	IP Reuse	System Testbench		
<i>Function Block</i>	RTL Synthesis	RTL Simulation		<i>Transistor Centric</i>
<i>Physical Implementation</i>	Place & Route	Timing, Signal, Yield Modeling		
	<i>Creation</i>	<i>Verification</i>		



Forecasting Multiple Processor SOC

More Processors

More Performance per Processor



Source: Network processor analysis by K. Keutzer, UCB