Implementing Low-Power Configurable Processors Practical Options and Tradeoffs

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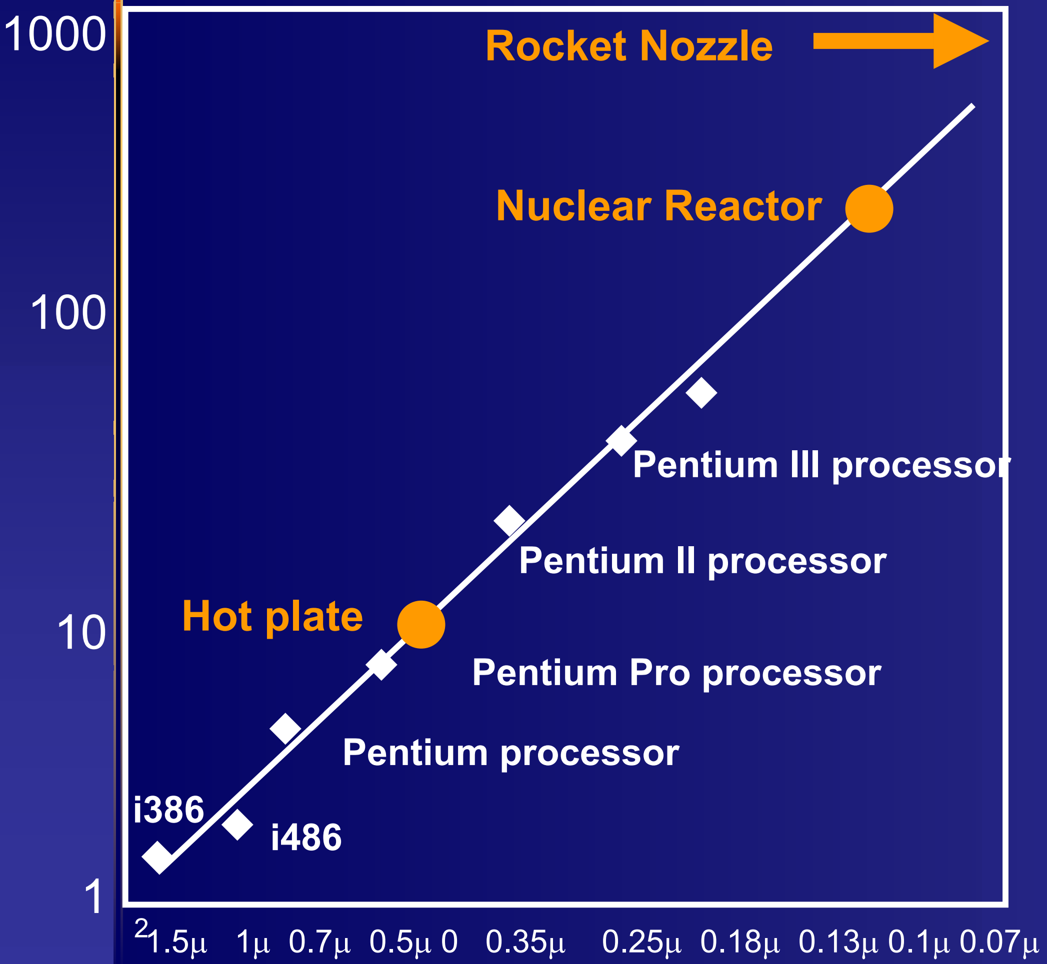
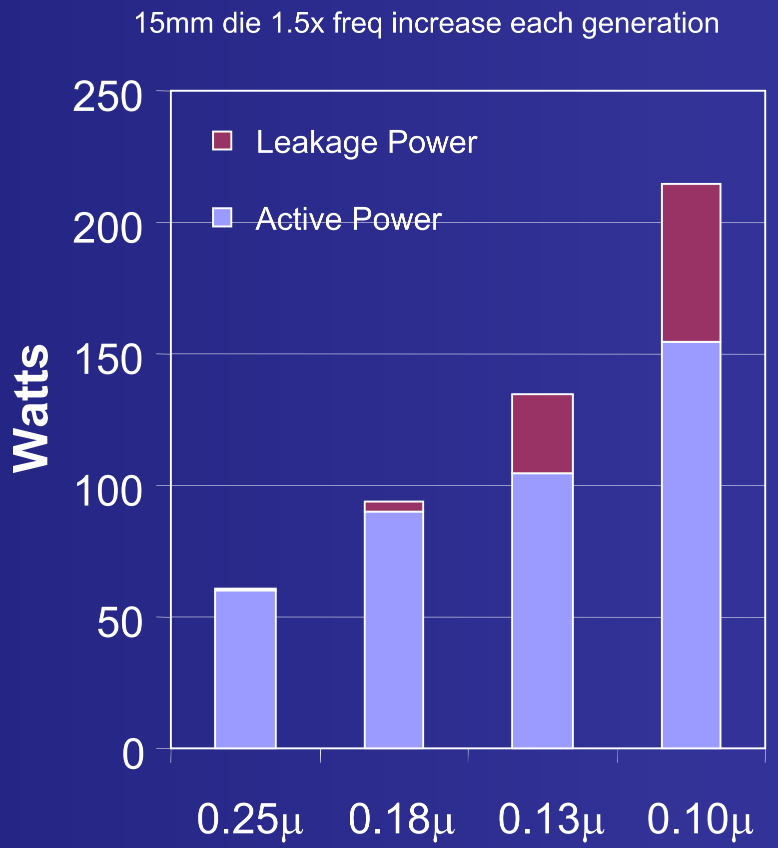
We Know All About Power

- Intel Projections:
- F. Pollack Micro32 1999



- Exponential growth in power in constant die size processors


15mm die 1.5x freq increase each generation

Power and Processors: Design Drivers for SoCs

- Power dissipation is one of the most important objectives in the design of embedded systems
- Power goals drive performance and cost of a SoC.
- Processors have emerged as fundamental building blocks for design of SoCs
  - Manage complexity afforded by Moore's Law
  - Manage time-to-market
  - Mitigate design and verification risks
  - Manage evolving protocols and standards
- What practical options exists to reduce power dissipated by a processor based solution?

The Energy Challenge

- The energy dissipated is as important as power for battery operated embedded systems for consumer applications
- Energy objective increases the design space, hence, design flexibility

$$E_{task} = (P_{dyn} + P_{leak})\ Time$$
$$= A\ C\ V^2\ N + P_{leak}\ N / f$$

Where E_{task} is energy of performing a computation task

P_{dyn} and P_{leak} are leakage and dynamic power respectively

A is effective switching activity (fraction of cap switched per cycle)

C is capacitance of the circuit

V is supply voltage

N is number of cycles to execute the computation task

f is clock frequency

Energy Reduction Approaches

- To reduce energy $E_{task} = A\ C\ V^2\ N + P_{leak}\ N\ /\ f$
- Reduce N: improve logic to execute task in fewer cycles - Architecture
- Reduce V: run circuits at lower voltage (which may mean lower frequency) - Circuit
- Reduce C: fewer transistors, smaller transistors, lower dielectric, smaller process geometry - Circuit
- Reduce A: more intelligent circuits to reduce unproductive switching (e.g. clock gating) - Circuit

Architecture Impact on Energy

- Architect the processor to fit the application
  - Acceleration using instruction extension
  - Gate-off clock to instruction extension hardware when not in use
- Energy optimization of processor
  - Increases power/cycle slightly
  - Reduces cycles/task significantly
  - Opens the door to voltage reduction

Architecture Impact on Energy: Case Studies

Four algorithms:

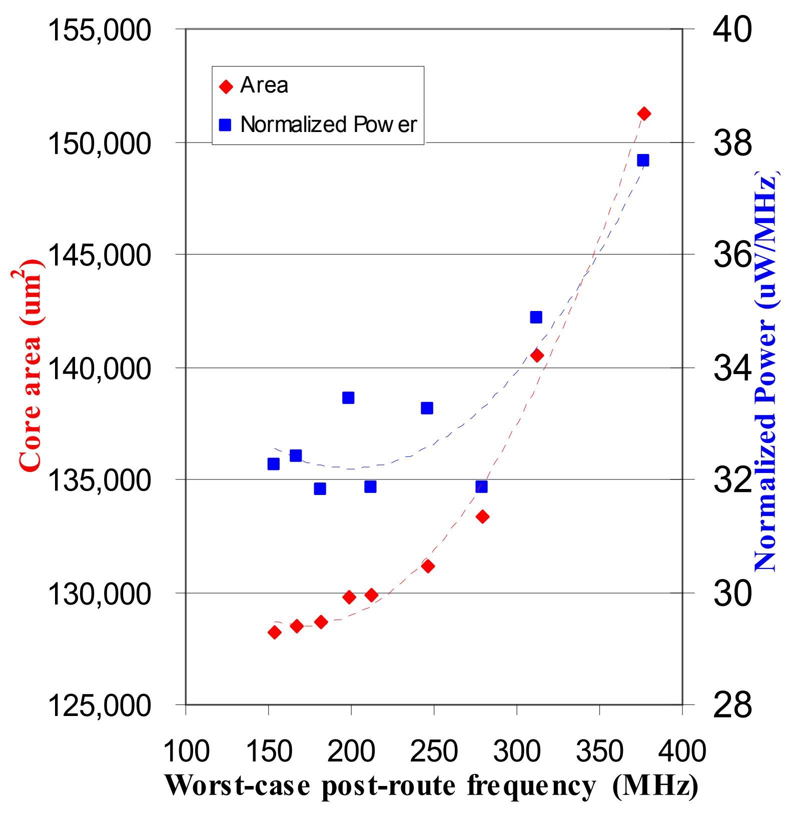
- dot-product (DotProd) of two 2048 element vectors
- Advanced Encryption Standard (AES) security coding
- Viterbi trellis decoding for wireless communication
- 256-point complex Fast Fourier Transform (FFT).

Config	Metric	DotProd	AES	Viterbi	FFT
Reference Processor	Area (mm^2)	0.9	0.4	0.5	0.4
	Cycles (K)	12	283	280	326
	Power (mW/MHz)	0.3	0.2	0.2	0.2
	Energy (μJ)	3.3	61.1	65.7	56.6
Optimized Processor	Area (mm^2)	1.3	0.8	0.6	0.6
	Cycles (K)	5.9	2.8	7.6	13.8
	Power (mW/MHz)	0.3	0.3	0.3	0.2
	Energy (μJ)	1.6	0.7	2.0	2.5
Energy Improvement		2	82	33	22

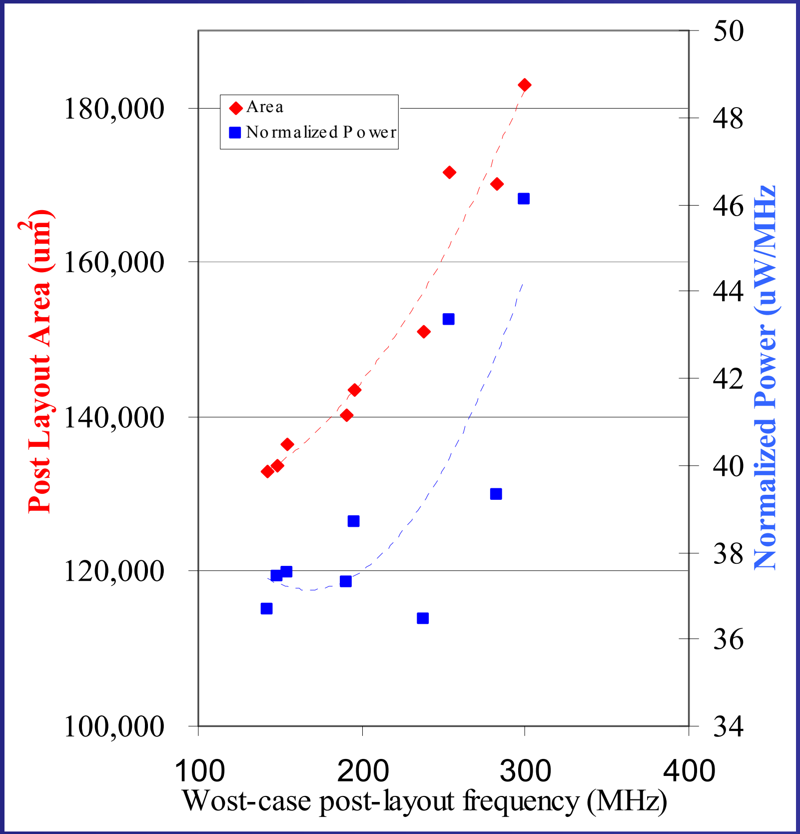
Circuit Impact on Energy

- Explore:
  - Is it possible to configure 32-bit processors for very small size and power?
  - How far can voltage be reduced while maintaining useful circuit performance?
  - What is the impact of process technology on power?
  - How significant is leakage compared with dynamic power?
  - What is the potential for dynamic voltage and frequency scaling?
- Method:
  - Choose a single small configuration
  - Apply best available synthesis, layout and standard cell library technology and optimize for a wide range of voltage and frequency targets
  - Target popular foundry technology: TSMC 0.13u GFSG and LVLK-OD process

Basic Speed-Area-Power Tradeoff



TSMC 0.13um LVLK-OD



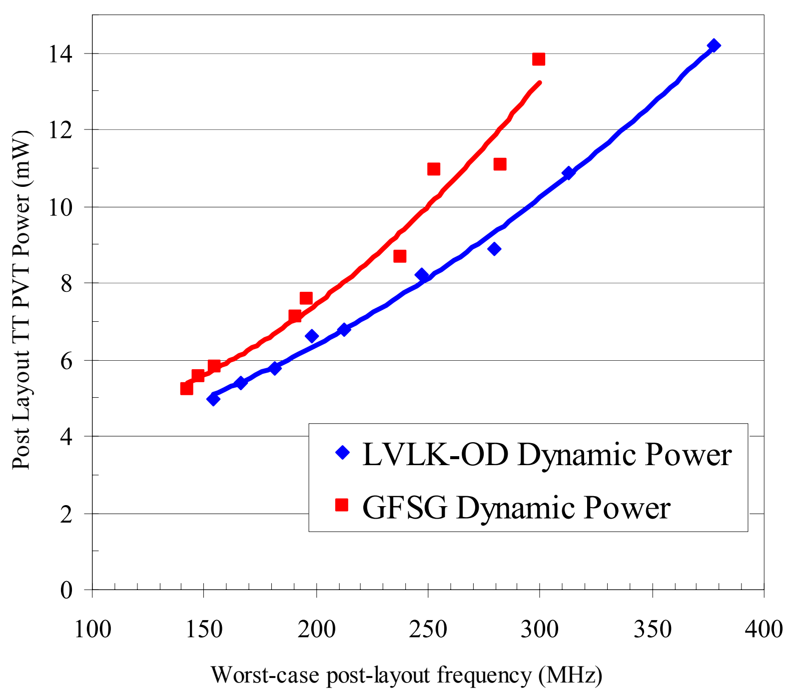
TSMC 0.13um GFSG

Artisan SAGE-X libraries

How fast should my design be?

- Dynamic power per MHz increases rapidly with target frequency beyond a certain frequency range
  - Why? Gate upsizing leads to increased capacitance
- Design guideline: ensure that target frequency is below the knee of the power curve
  - Side benefit: smaller area and smaller leakage power
- Scaling down processor frequency to reduce power is enabled by custom instruction-based application code acceleration

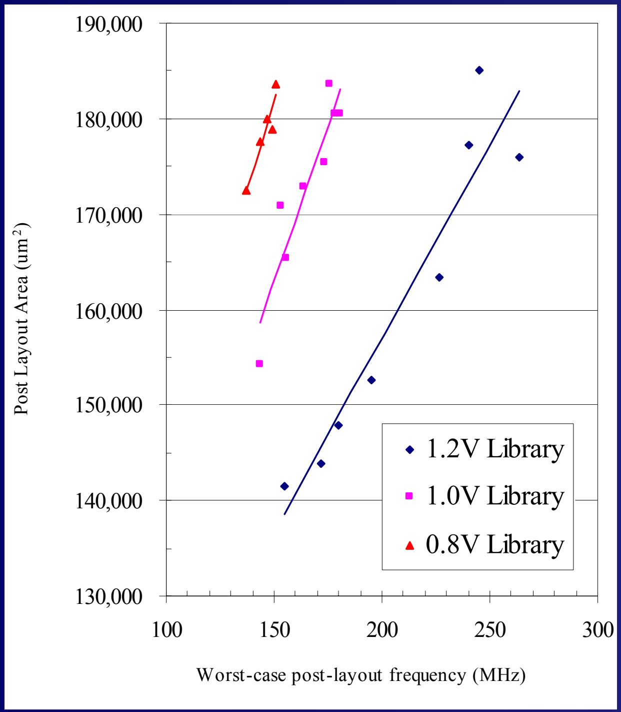
Impact of Process Technology

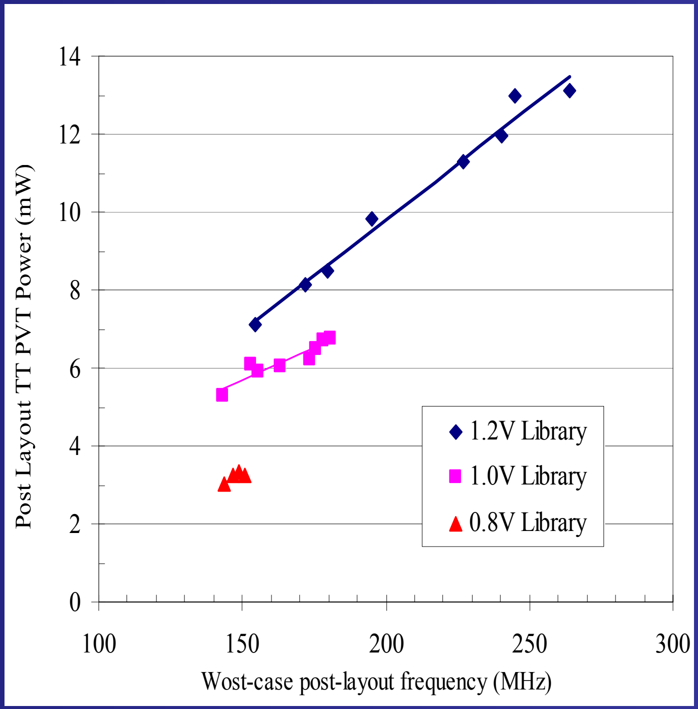


- LVLK-OD has lower dynamic power than GFSG across broad target frequency range
- More than 440% increase in leakage for LKLV-OD (0.169 mW) compared to GFSG (0.031 mW)
- Total power savings using 0.13 μm LVLK-OD is at least 10% from 150MHz through 300 MHz with savings diminishing at lower speed
- Power-aware process selection requires analysis of total power for target frequency range

Scale Voltage to Match Frequency Goals

- Low voltage design does need more area: synthesis up-sizes gates to get enough drive
- Power/cycle reduced by ~V^2 as expected: 3 mW for high-performance processor core @ 0.8 V

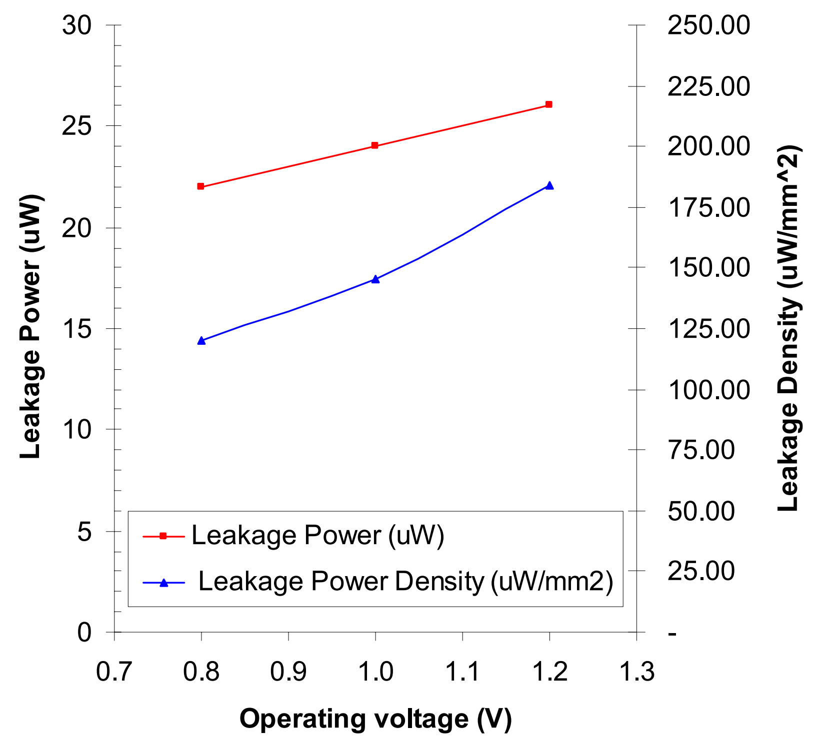




Xtensa Processor Implemented using Virtual Silicon Mobilize library

Leakage: 150MHz Cores with Voltage Scaling

- Leakage per area declines with voltage
- The decline in leakage power density is much sharper than the decline in the leakage power
- Total leakage for 150 MHz target declines less sharply due to larger gates at lower target voltage

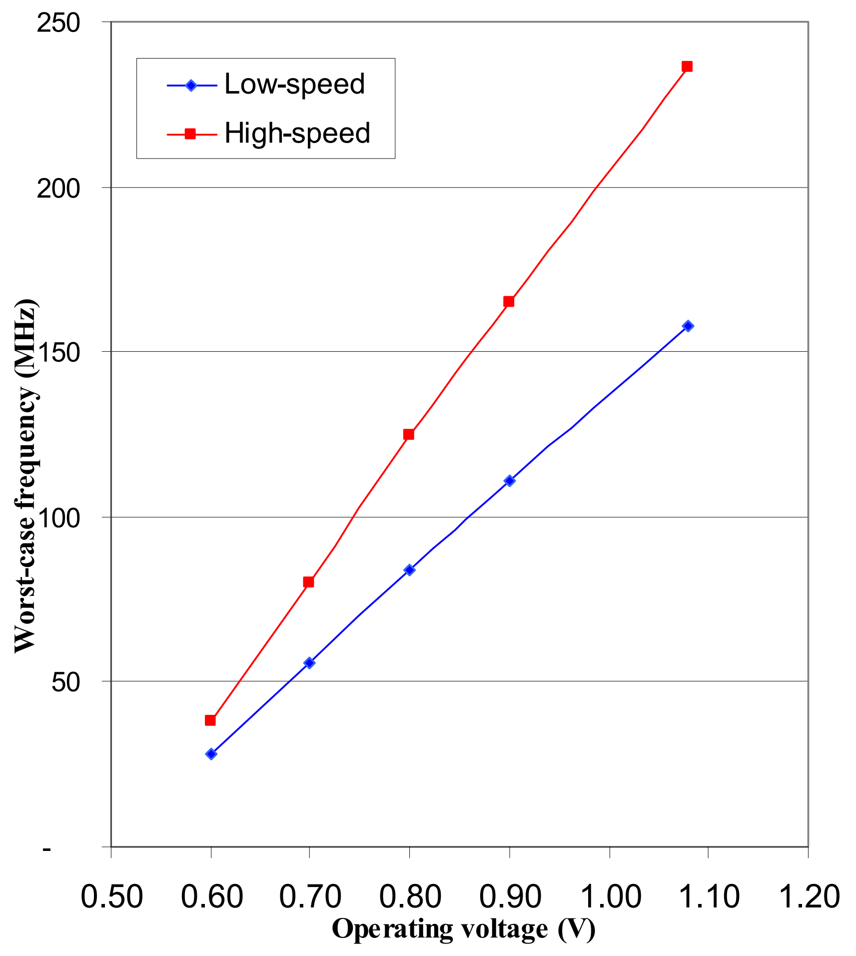


Leakage Power and Leakage Density (TT process corner)

Xtensa Processor Implemented using Virtual Silicon Mobilize Library

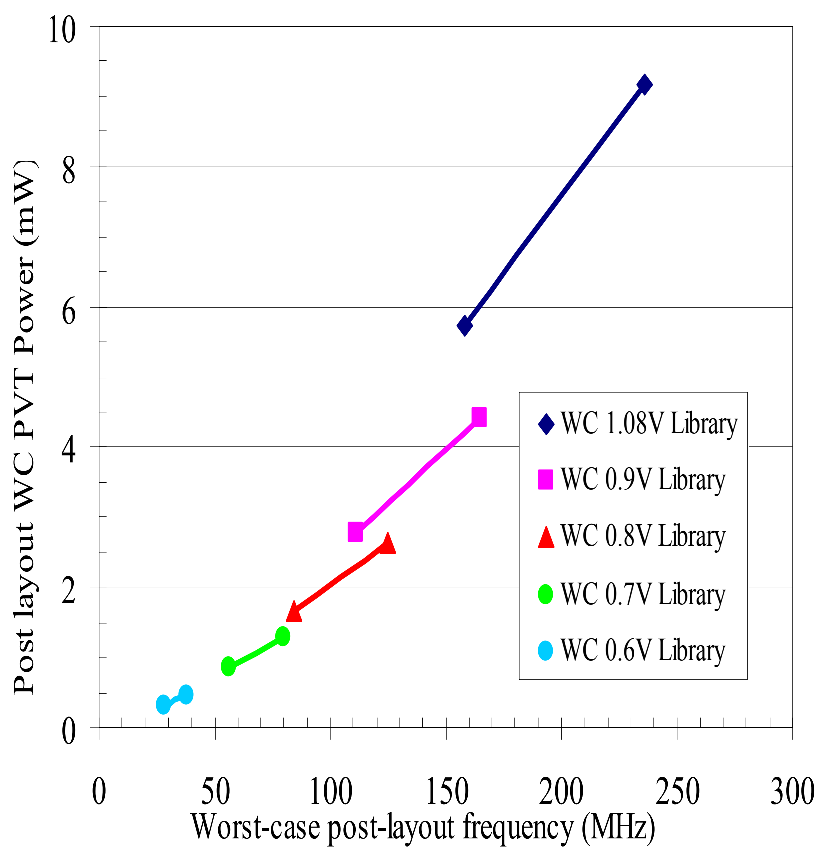
Aggressive Voltage Scaling for Best Energy

- Scale small processor to 0.6V using Artisan METRO™ standard cell libraries
- Two variations synthesized with 1.08V library:
  - maximum speed (0.15mm^2)
  - minimum area and power (0.12mm^2)
- Re-characterized for each voltage point
- F_{max} scales with voltage
- Still have useful frequency at 0.6V (30-40MHz worst case), especially with processor extension



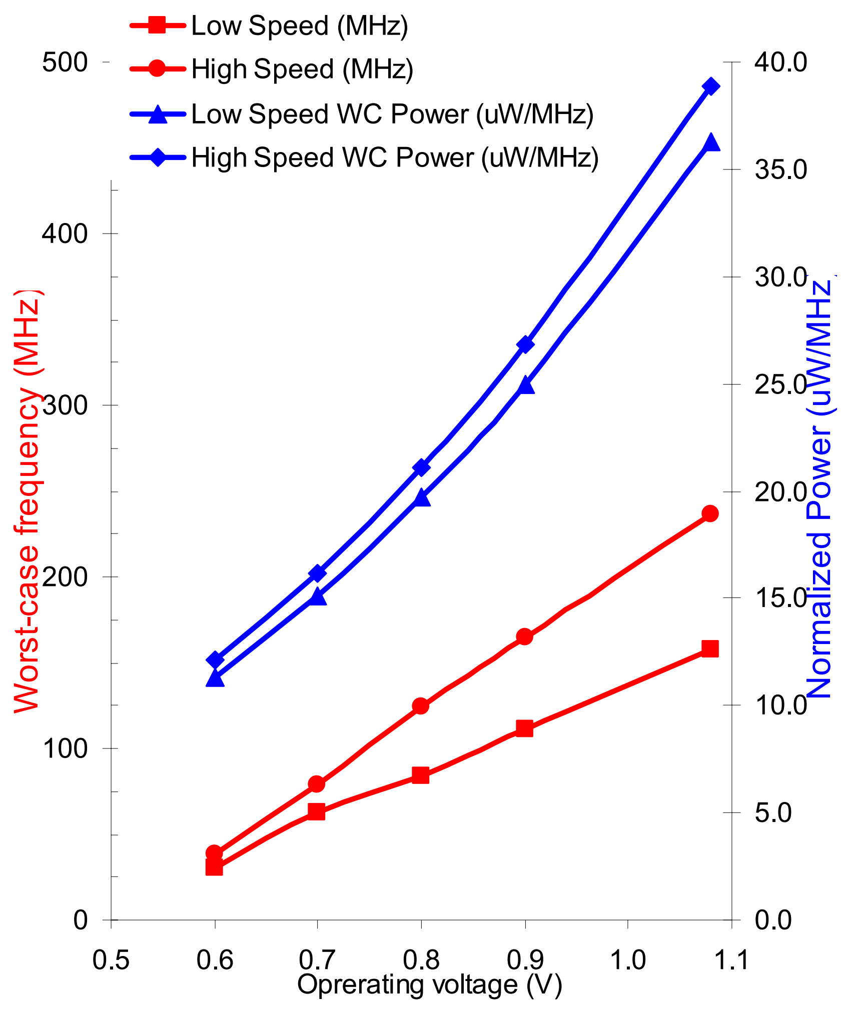
Wide Operating Range Maximizes Energy Efficiency

- Xtensa processor implemented using Artisan METRO™ libraries
- Large power savings when the same processor design downshifts to lower V while also operating at a lower clock frequency



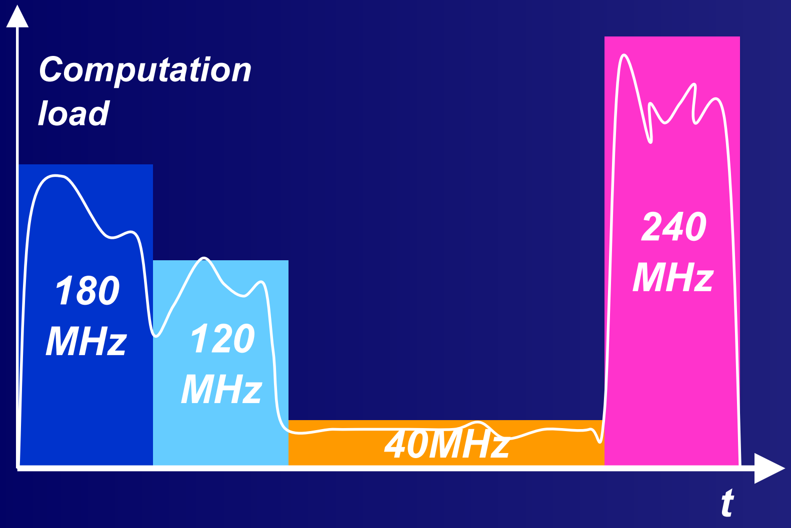
Max Speed vs. Min Area Optimization

- Optimizing for speed gives significant frequency boost (30-50%) for small power increase (<10%)

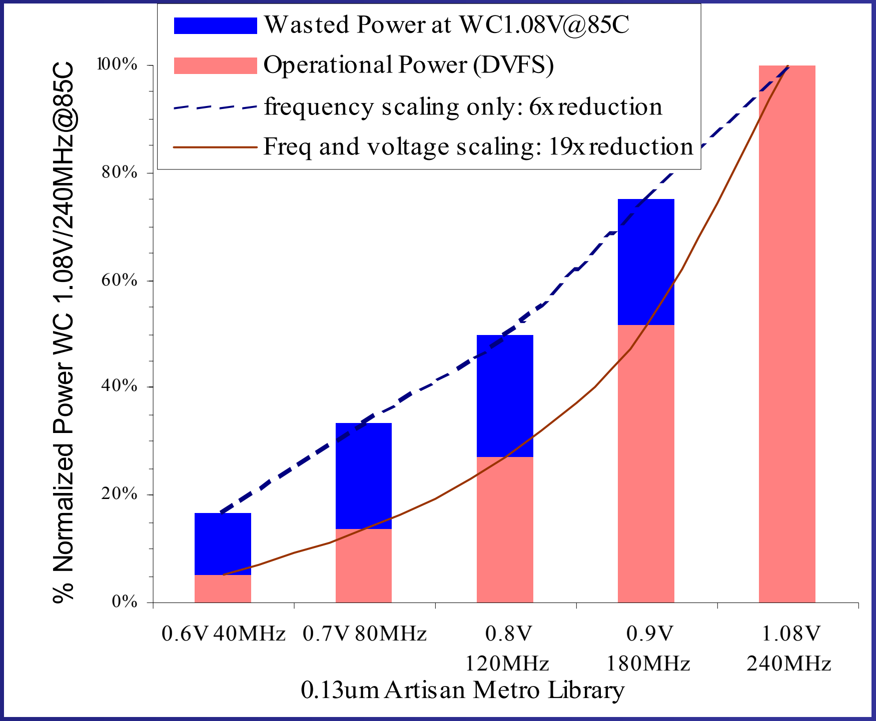


Dynamic Voltage and Frequency Scaling

- When process runs tasks with know throughput requirements, pick lowest frequency (and voltage) that get job done just in time.
- When work-load is changing or unpredictable, adjust frequency (and voltage) to meet changing needs: DVFS

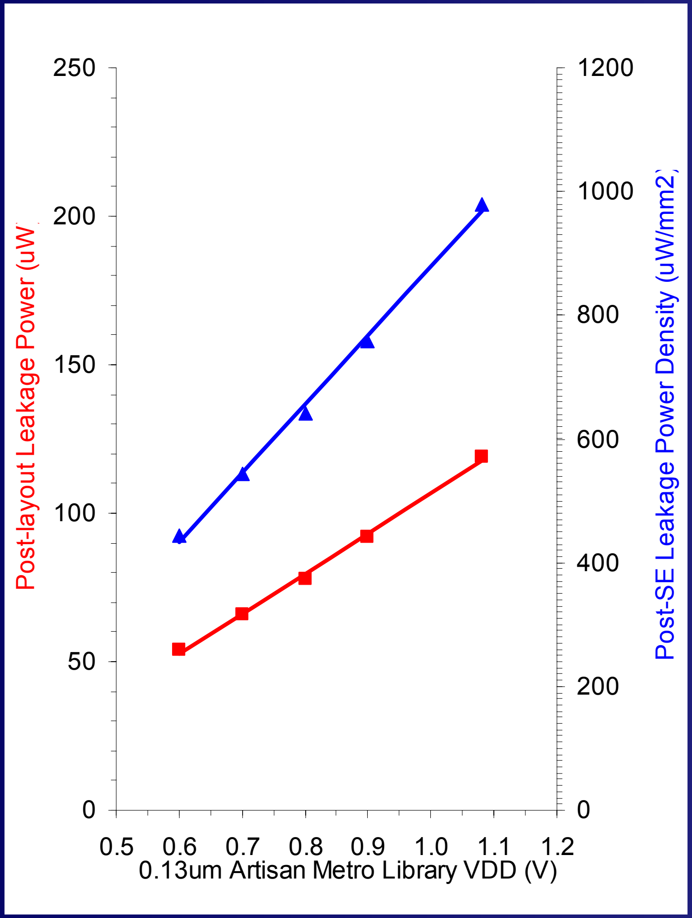


- F_{max} vs Voltage characterization sets potential energy savings for 240MHz down to 40MHz range
- Frequency scaling only 6x energy reduction
- Frequency and voltage scaling: 19x energy reduction

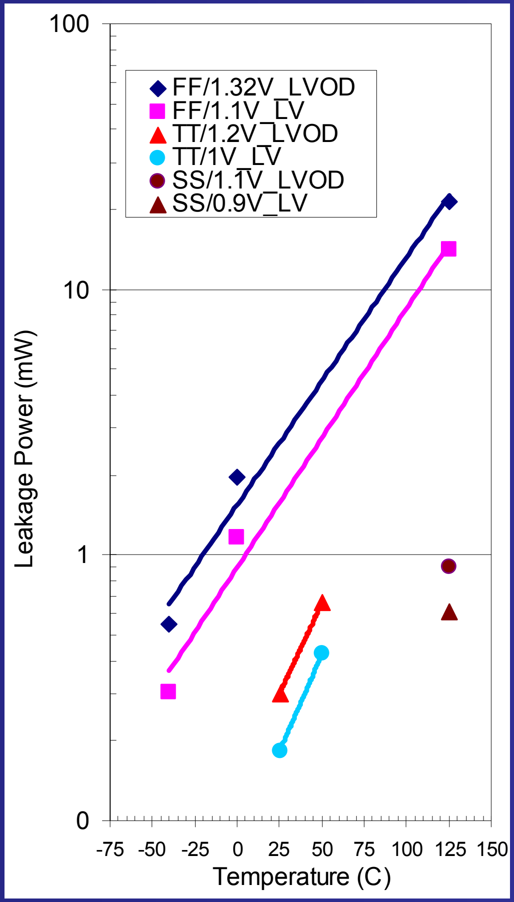


Leakage Issues in Processor

Voltage



Temperature



Artisan METRO™ Standard Cell Libraries

Conclusion

- Power is an increasingly important design objective
- Processors are emerging as a key building blocks for designing SoCs
- The design challenge is to explore the practical power reduction techniques for processor oriented solutions
- We examine effect of and interrelationship among the following factors that affect the power
  - processor architecture (instruction extensions)
  - speed objective
  - area objective
  - process technology
  - low voltage libraries