



# ConnX Turbo16MS

## Multi Standard Turbo Decoder – Hardware Performance, Software Flexibility

### Product Brief

#### FEATURES

- 3GPP-HSPA+ specification turbo decoding
  - Supports all block sizes from 40 to 5114 bits
  - Supports 85 Mbps decoding with 8 full iterations (operating frequency of 385 MHz)
  - Extrinsic log-likelihood ratio (LLR) based early termination for reduced power operation
- 3GPP LTE specification turbo decoding
  - Supports all block sizes from 40 to 6144 bits
  - Supports 150 Mbps with 8 full iterations (operating frequency of 385 MHz)
  - Code block CRC-based early termination for reduced power operation
- Block-by-block change of physical layer mode (HSPA+/LTE), block length, and number of iterations
- 8-window based parallel decoding, with option of 4/2/1 window parallel decoding for smaller block length codes
- One cycle per 16 bits for each ALPHA/ BETA update
- 6-bit precision for input LLR
- Confidence accumulation functionality supports early termination

#### BENEFITS

- LTE turbo decoding of up to 150 Mbps data streams with 8 full iterations
- HSPA+ Turbo decoding of up to 85 Mbps data streams with 8 full iterations
- Small size and low power
  - Single processor with software programmability allows multi-standard turbo decoder implementation
- Support for cycle and power reduction by early termination
- Software programmability to support multiple I/O formats
- Road map to encompass future evolutions of the LTE/HSPA+ standard
- C-code programming model with full development tool chain support speeds development

#### Enormous Computation Performance for Multi-Standard (LTE and HSPA+) Turbo Decoding

The ConnX Turbo16MS is a high-performance dataplane processor unit (DPU) specifically designed for decoding of LTE Turbo codes on data streams of up to 150 Mbps and HSPA+ data streams of up to 85 Mbps. This performance is required for 3.9G and 4G cellular radios and multi-standard broadcast receivers.

ConnX Turbo16MS is based on Tensilica's Xtensa® processor and has been optimized in two areas. First, a customized single cycle execution instruction set has been developed for LTE and HSPA+ turbo decoding. Second, it uses parallel execution for very high data bandwidth computation. This includes the 5-issue VLIW capability and the two load/store units that allow loading of dual memories in a single cycle. There are also 23 very tightly coupled scratch pad memories for storing a priori and state values that are accessed by instructions in parallel. This results in up to five memory accesses per cycle. Only this level of parallelism can give ConnX Turbo16MS the performance needed for multi-standard turbo decoding.

Some of the key architecture features include:

- 5-issue VLIW for efficient parallel operations
- Dual 128b load/store units
- Optimized register files for turbo decoding
- Dedicated TIE Lookup memory for a priori and state values

The ConnX Turbo16MS uses two MAP decoders. Each decoder performs two passes on the data. This is done with an 8-window scheme operated in parallel, with two bits per cycle. The operation of the MAP decoders is controlled by instructions, with data being loaded in parallel for execution in the 16-way SIMD engine. Interleaving and de-interleaving is performed at the same time as memory reads or writes.

Because ConnX Turbo16MS is a processor, software algorithms can be altered to suit specific customizations in performance and input-output format as needed. Optimized software for HSPA+ and LTE is provided and is free for customer modification and use.



### Small Size

	Cell area (post synthesis) (mm <sup>2</sup> )	Cell and Routing area (post place and route) (mm <sup>2</sup> )	TOTAL AREA Core (cell and routing) and Memory (mm <sup>2</sup> )
45GS	0.52	0.80	1.62
40LP	0.67	1.03	1.73

Memory Instance	Size
Instruction Memory	16 KB
Dual Data Memory	64 KB
State Memory Bank	28.5 KB
Interleave Memory Banks	9 KB
DecBits Memory Bank	0.8 KB
<b>TOTAL</b>	<b>118.3 KB</b>

### Low Power

Power Consumption (mW) for ConnX Turbo16 Core / Memory @ 385MHz

Technology	Specification— Mbps	8 Iterations	6 Iterations	4 Iterations
40 LP	LTE 150	205.5 / 51	154 / 39	106 / 27
40 LP	HSPA+ 85	147 / 35	112 / 27	79 / 18.5
45 GS	LTE 150	113 / 46.5	84.5 / 35.5	58.5 / 24.5
45 GS	HSPA+ 85	79.5 / 33.5	60.5 / 26	43 / 18

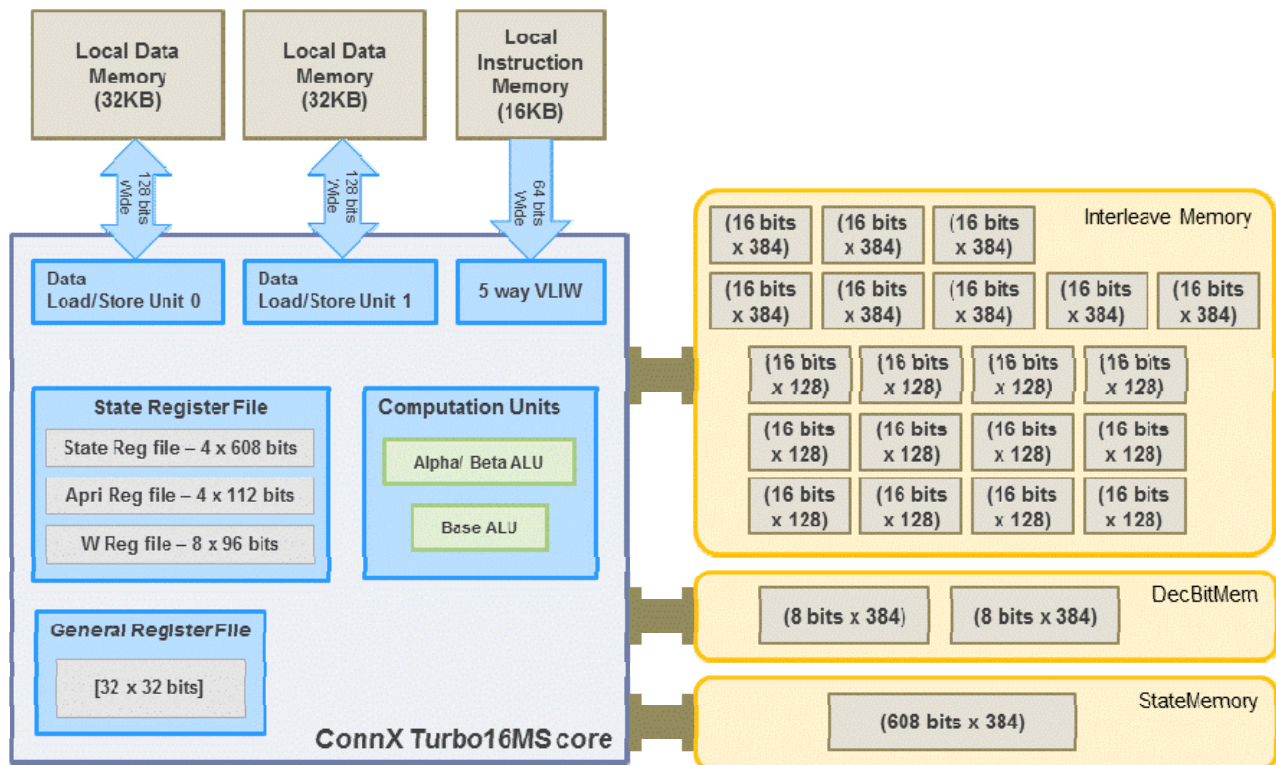


Figure 1. A simplified diagram of the architecture of the ConnX Turbo16MS Turbo Decoder

### Programming Model

ConnX Turbo16MS is a highly optimized dataplane processor for turbo decoding. To enable a customer to quickly use this processor, a library is provided. The library contains API functions for LTE and HSPA+, which performs the fundamental Turbo block decode operation. This function can be called by the customer's higher level algorithm, implementing the turbo decoding system block.

### Toolchain

The ConnX Turbo16MS comes with a complete set of simulation and debug tools. A comprehensive instruction set simulator (ISS) allows developers to

quickly simulate and evaluate performance. It is integrated into System C (XTSC) transaction-level and pin-level system modeling to enable simulation of the ConnX Turbo16MS core and memories.

The toolset includes a high-performance C/C++ compiler with support for automatic issue of pipelined VLIW instructions. This comprehensive tool set also includes the linker, assembler, debugger, profiler, an energy estimation tool and graphical visualization tools. All major back-end EDA flows are supported for different geometries and process technologies.

Native simulation using C-Stub can enable easy integration of the software model of Turbo16MS into a larger overall C/C++ system model.

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