



# Diamond Standard 570T Controller

## A 3-Issue VLIW CPU Core

### Product Brief

#### FEATURES

- Two- or three-issue Very Long Instruction Word (VLIW) CPU
- Modeless switching between 16-, 24- and 64-bit instructions keeps code size low
- Compiler automatically creates VLIW instructions
- Dhrystone 2.1: 1.59 DMIPS/MHz
- Dual 32x32 MULs and 32-bit integer divider
- 16-bit DSP instructions
- 16Kbyte, 2-way set associative instruction and data caches, programmable write-through and write-back
- Single-cycle instruction and data SRAM interface
- High-speed XLMI peripheral port
- Memory protection unit
- 64-bit PIF interface
- 2x32-wire GPIO ports for direct control and monitoring of peripherals
- 2x32-bit Queue interfaces for streaming data into and out of the processor via FIFOs
- On-chip debugging hardware
- Embedded trace support
- AHB-lite and AXI bridges

#### BENEFITS

- High performance, low area CPU
- Simple programming model—Compiler automatically maps C/C++ to SIMD and VLIW to boost performance
- High arithmetic and DSP performance, reducing need for separate DSP
- Fast and flexible interrupt handling
- Bypass system bus and communicate directly via GPIO and FIFO interfaces
- Drop into existing AMBA™-based SOCs

#### Ultra High Performance CPU with DSP

The Diamond Standard 570T is Tensilica's fastest standard controller and includes DSP instructions to help eliminate the need for a co-processor.

#### When You Need Performance

The Diamond Standard 570T is among the highest performance, highest throughput licensable CPUs available today. It combines an efficient 5-stage pipeline with a 3-issue VLIW architecture, enabling it to obtain leading performance levels on both control and DSP code.

Due to the Diamond 570T's flexible base architecture, 16-, 24-, and compound 64-bit VLIW instruction bundles can be freely intermixed in the instruction stream with no processor mode switching, thus maintaining performance while optimizing code size. The compiler automatically creates 64-bit VLIW instruction bundles if instructions can be issued simultaneously; otherwise, a single 16/24-bit instruction is issued. This capability increases code density to industry leading levels, reducing the amount of on-chip cache or memory required for storage of instructions.

The Diamond 570T includes many standard DSP instructions that increase the performance of numerically intensive applications, plus a 32x32 multiplier and 32-bit integer divider. Example DSP instructions include: zero overhead looping, clamps (saturating arithmetic), max/min value, normalize, and sign extend. Additionally, a MAC unit enables high performance on inner loops requiring fast multiply accumulate operations.

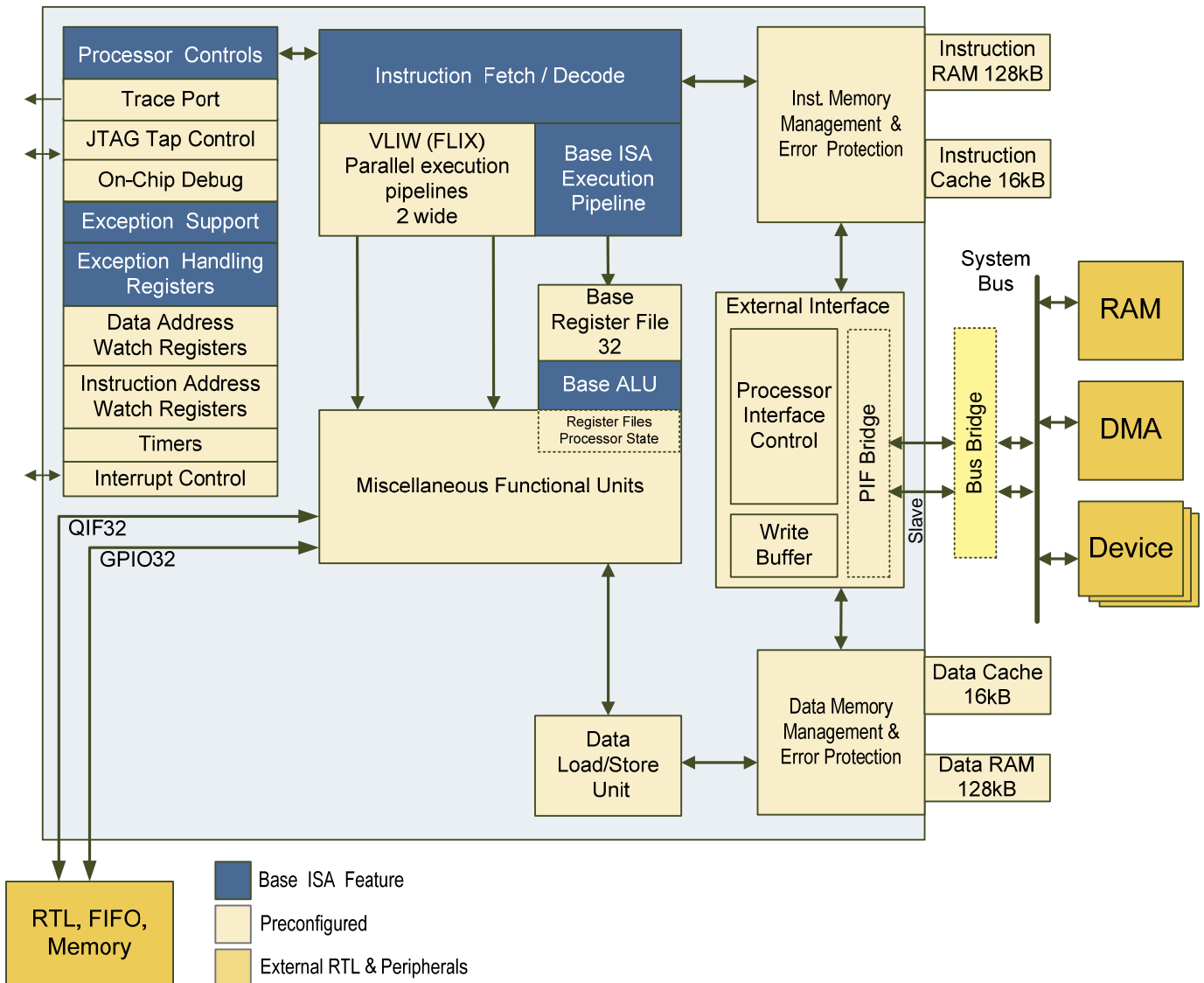
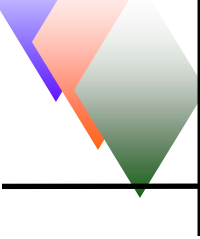
The Diamond 570T features innovative I/O that allows data to be streamed in and out of the processor without going over the main data bus. The two 32-wire GPIO (general-purpose I/O) ports allow direct control and monitoring of peripherals. Two 32-bit FIFO port interfaces can connect to standard FIFOs for direct, predictable communication with other RTL blocks, devices and processors.

#### Instruction Set Architecture

The Diamond Standard Series implements the Xtensa® Instruction Set Architecture (ISA) a 32-bit RISC architecture featuring a compact instruction set optimized for embedded designs.

The Xtensa ISA employs 24-bit instructions with 16-bit narrow encodings for the most common instructions. These 16- and 24-bit instruction words are freely intermixed to achieve higher code density without compromising application performance.





### The Diamond Standard 570T

#### Instruction Set Architecture (cont.)

The Xtensa ISA thus optimizes the size of the program instructions by minimizing both the static number of instructions (the instructions that constitute the application program) and the average number of bits per instruction.

The use of 24- and 16-bit instruction words and compound instructions, the richness of the comparison and bit-testing instructions, zero-overhead-loop instructions, register windowing, and the use of encoded immediate values all contribute to the Diamond processors' small code size. The 24-/16-bit Diamond

processor ISA enables designers to achieve 25% to 50% lower code size compared to conventional 32-/16-bit ISA-based RISC cores.

Reducing code size results in smaller memory sizes and lower power dissipation – key parameters in cost-sensitive, highly integrated SOC designs.

The Xtensa ISA also provides powerful compare-and-branch instructions, zero-overhead loops, and bit manipulations including funnel shifts and field-extract operations.





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## Comprehensive Software Tool Support

A full-featured development environment – the Xtensa Xplorer™ – provides a graphical user interface (GUI) to all code development tools. The compiler toolchain and instruction set simulator (ISS) are available through the GUI in addition to performance modeling tools. Based on the Eclipse framework, Xtensa Xplorer allows developers to quickly evaluate code on the pipeline-accurate ISS and interface to emulation and hardware development boards. Xtensa Xplorer serves as the cockpit for the entire development .

Tensilica's XCC C/C++ compiler is an optimizing compiler that employs sophisticated multi-level optimizations to increase code

execution performance and reduce code size. Also included in the Xtensa Xplorer environment are a software project manager, code profiling tools, source code editor, debugger, performance-modeling tool, the Xenergy™ energy estimation tool, the cache performance explorer, and a number of graphical visualization tools. Tensilica also provides both a C-based modeling environment called XTMP, as well as SystemC models of the Diamond processors. For fast-functional simulation, Tensilica offers TurboXim for a 40-80x faster simulation than the ISS. See Tensilica's Software Developer's Toolkit product brief for more information.

## Specifications

	65gp		65lp		45gs		40lp	
Flows:	High-Speed	Low-Power	High-Speed	Low-Power	High-Speed	Low-Power	High-Speed	Low-Power
Post-route cell area (mm <sup>2</sup> )	0.440	0.257	0.463	0.249	.283	0.158	0.295	0.163
Speed (MHz) post Prime Time	635	58	399	57	780	58	493	57
Post-Route Power (mW/MHz)	0.110	0.058	0.142	0.080	0.066	0.034	0.093	0.046

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