



ConnX 545CK DSP

8-MAC VLIW DSP Core

Product Brief

FEATURES

- High performance and efficiency for DSP operations
- 3-issue VLIW with 8-way SIMD units
- Compiler automatically vectorizes code
- DSP instructions native to single core, modelessly switching between 16-, 24- and 64-bit instructions
- Dual 128-bit load/store units
- Eight 16-bit MACs that operate in SIMD mode
- 32-bit input/output Queue (FIFO-like) interfaces
- Viterbi convolutional coder accelerator
- AHB-lite and AXI bridges

BENEFITS

- Very high and flexible computational performance
- Performance headroom allows operation at lower frequency to reduce power consumption
- Single core, single development environment due to native DSP instructions
- Ideal for communication baseband applications
- Very high I/O throughput; higher than XY DSPs
- Bypass system bus and communicate directly via Queue interfaces
- Drop into existing AMBA™-based systems

Part of Tensilica's ConnX Family of High-Performance DSPs

The ConnX 545CK is an important member of Tensilica's ConnX family of DSPs, which ranges from the 2-MAC ConnX D2 up to the 16-MAC ConnX Baseband Engine (BBE16). Please visit our web site to review all of the capabilities of these high-performance DSPs.

High Performance DSP Core

The ConnX 545CK is one of the highest performance licensable DSP IP cores. The ConnX 545CK allows system control and industry leading data processing throughput in a single core with a single compiler and single instruction stream. It combines a base CPU controller with a DSP containing eight parallel 16-bit MAC units, allowing it to sustain eight simultaneous MAC operations on independent data pairs per cycle, utilizing the 160-bit vector registers.

As in all Xtensa® ISA-based architectures, 16-, 24- and 64-bit VLIW instruction bundles are freely intermixed in the instruction stream with no processor mode switching to decrease performance. All software development tools (compiler, linker, debugger, instruction set simulator) have been enhanced to enable access to DSP-related and control hardware through standard C/C++ source code.

In addition to the data processing gains realized through parallel multiplier hardware, the ConnX 545CK includes support for other DSP-related operations, such as zero-overhead looping, clamps (saturating arithmetic), max/min value, normalize, and sign extend.

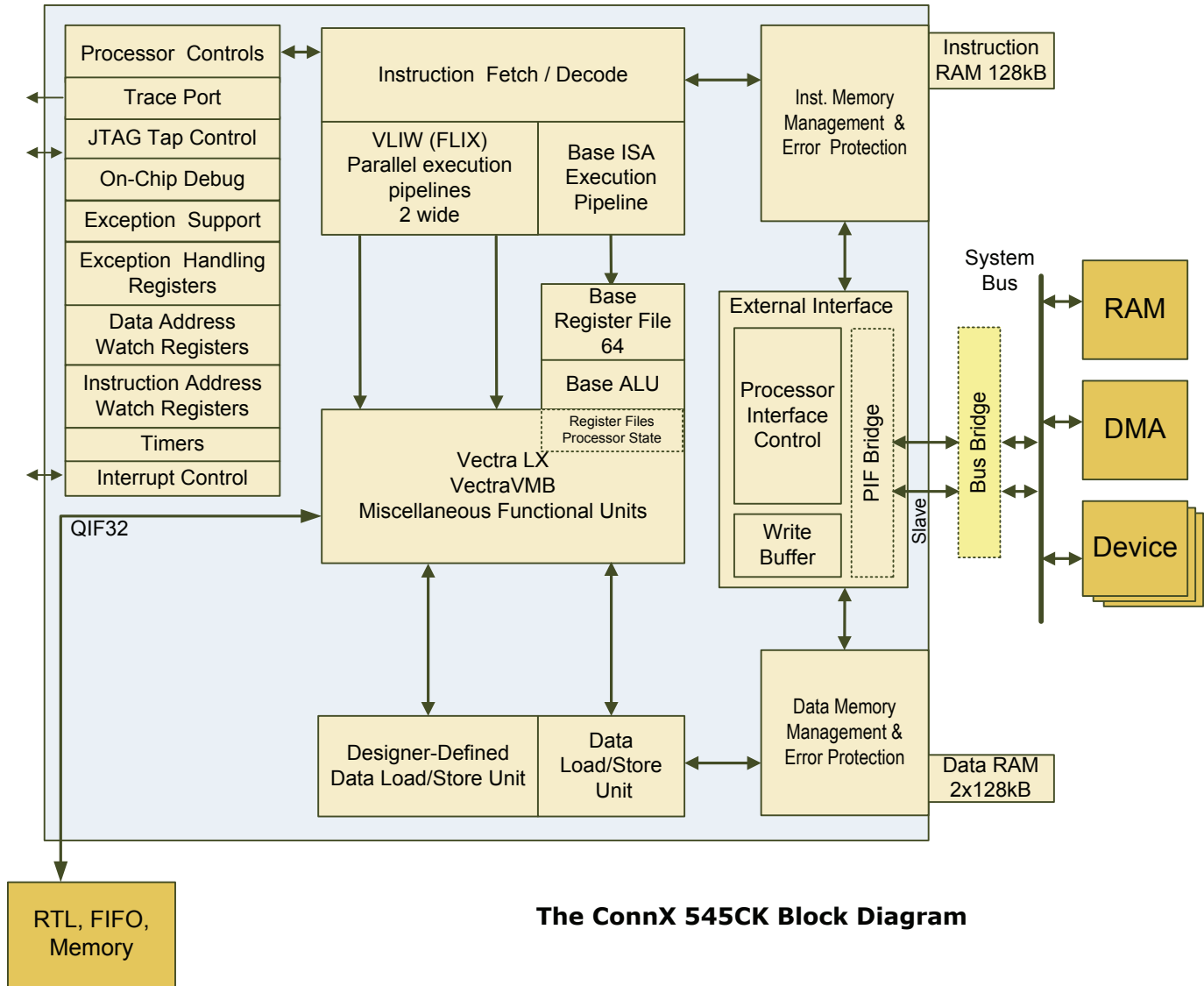
The ConnX 545CK is an industry leading combination of an efficient 32-bit RISC controller and an extremely high-performance DSP in a single licensable IP core. It eliminates or greatly reduces the need to develop SOCs with separate control and DSPs.

Instruction Set Architecture

The ConnX 545CK implements the Xtensa Instruction Set Architecture (ISA), a 32-bit architecture featuring a compact instruction set optimized for embedded designs. The architecture has a 32-bit ALU, 32 general-purpose physical registers, 6 special-purpose registers, and 80 base instructions, including compact 16- and 24-bit (rather than 32-bit) RISC instruction encoding. This reduces code size 10% to 40% compared to conventional RISC cores, depending on the actual code. Reducing code size results in higher performance, smaller memory sizes, and better power dissipation.

The Xtensa ISA's 16- and 24-bit encoding also provides powerful branch instructions, zero-overhead loops, and bit manipulations including funnel shifts and field-extract operations. This architecture is extended with 64-bit VLIW "bundles" - which are composed of multiple instructions—for the ConnX 545CK processor. Tensilica's XCC C/C++ compiler generates an optimized combination of 16-, 24- and 64-bit instructions in a single instruction stream, so there's no CPU mode switching between different types. Firmware developers do not need to





The ConnX 545CK Block Diagram

decide which parts of their code should be compiled with different length instruction encodings.

Comprehensive Software Tools Support

A full-featured development environment – the Xtensa Xplorer™ – provides a graphical user interface (GUI) to all code development tools. The compiler toolchain and instruction set simulator (ISS) are available through the GUI in addition to performance modeling tools. Based on the Eclipse framework, Xtensa Xplorer allows developers to quickly evaluate code on the pipeline-accurate ISS and interface to emulation and hardware development boards. Xtensa Xplorer serves as the cockpit for the entire development .

Tensilica's XCC C/C++ compiler is an optimizing compiler that employs sophisticated multi-level optimizations to increase code execution performance and reduce code size. Also included in the Xtensa Xplorer environment are a software project manager, code profiling tools, source code editor, debugger, performance-modeling tool, the Xenergy™ energy estimation tool, the cache performance explorer, and a number of graphical visualization tools. Tensilica also provides both a C-based modeling environment called XTMP, as well as SystemC models of the ConnX 545CK DSP. For fast-functional simulation, Tensilica offers TurboXim for a 40-80x faster simulation than the ISS. See Tensilica's Software Developer's Toolkit product brief for more information.



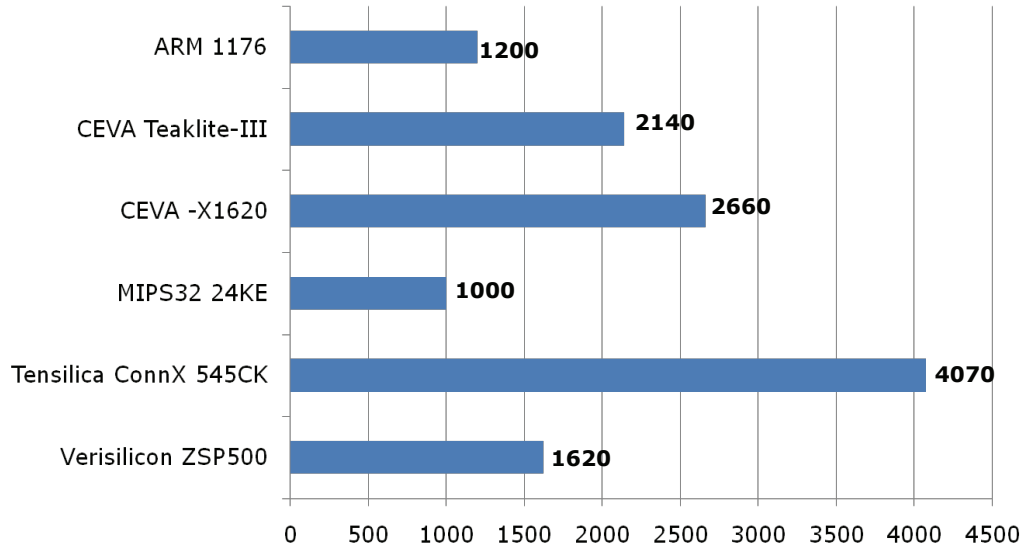
Selected Benchmark Comparisons

Tensilica's ConnX 545CK was certified by Berkeley Design Technology, Inc. (BDTI) to have achieved a BDTI speed score of 4070. All processors benchmarked with 16-bit fixed-point data. All scores use worst-case clock speeds for the TSMC CL013G process and ARM Artisan SAGE-X library. Vendors can choose different speed/area/power trade-offs; to understand

the trade-offs, please view all BDTI metrics for each core.

BDTIsimMark2000™ scores may be based on projected clock speeds. For information, see www.BDTI.com/benchmarks.html

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BDTI Speed Scores for Fixed-Point Licensable Cores

Specifications

Flows:	65gp		65lp		45gs		40lp	
	High-Speed	Low-Power	High-Speed	Low-Power	High-Speed	Low-Power	High-Speed	Low-Power
Post-route cell area (mm²)	1.04	0.65	1.116	0.645	0.688	0.395	0.705	0.403
Speed (MHz) post Prime Time	623	58	376	58	684	58	457	57
Post-Route Power (mW/MHz)	0.129	0.076	0.183	0.106	0.082	0.045	0.113	0.064

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