



FEATURES:

- Highest performance and efficiency of any licensable DSP core
- 3-issue VLIW DSP with 8-way SIMD units
- Compiler automatically vectorizes code
- DSP instructions native to single core, modeless switching between 16-, 24- and 64-bit instructions
- Dual 128-bit load/stores
- Eight 16-bit multipliers that operate in SIMD mode
- 16-entry, 160-bit-wide vector register file
- Two 128-bit load/store units
- 32-bit input/output FIFO interfaces
- Viterbi convolutional coder accelerator
- AHB-lite and AXI bridges

BENEFITS:

- Very high and flexible computational performance
- Performance headroom allows operation at lower frequency to reduce power consumption
- Single core, single development environment due to native DSP instructions
- Ideal for communication baseband applications
- Very high I/O throughput; higher than XY DSPs
- Bypass system bus and communicate directly via FIFO interfaces
- Drop into existing AMBA™-based systems

The Diamond Standard 545CK is the highest performance licensable DSP IP core. The Diamond 545CK, which combines a base CPU controllers and a DSP containing eight parallel 16-bit single-cycle MAC units, allows system control and industry leading data processing throughput in a single core with a single compiler and single instruction stream. The Diamond 545CK can sustain eight simultaneous MAC operations on independent data pairs per cycle, utilizing the 160-bit vector registers.

As in all Xtensa ISA-based architectures, 16-, 24- and 64-bit VLIW instruction bundles can be freely intermixed in the instruction stream with no processor mode switching to decrease performance. All software development tools (compiler, linker, debugger, instruction set simulator) have been enhanced to enable access to DSP-related and control hardware through standard C/C++ source code.

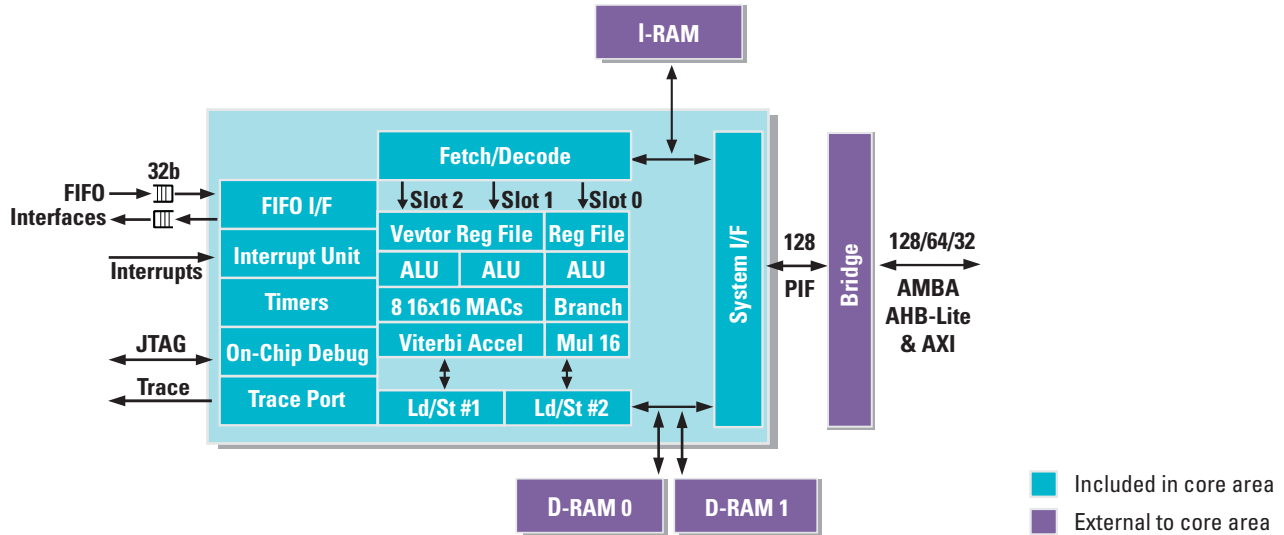
In addition to the data processing gains realized through parallel multiplier hardware, the Diamond 545CK includes support for other DSP-related operations, such as zero-overhead looping, clamps (saturating arithmetic), max/min value, normalize, and sign extend.

The Diamond 545CK is an industry leading combination of an efficient 32-bit RISC controller and an extremely high-performance DSP in a single licensable IP core. It eliminates the need to develop SOCs with separate control and DSPs.

Representative Performance/Area/Power	130G		90G		65GP	
	Speed Optimized	Area Optimized	Speed Optimized	Area Optimized	Speed Optimized	Area Optimized
Area (mm ²) post-synthesis	2.48	2.22	1.29	1.09	0.805	0.658
Cell area (mm ²) post-layout	3.58	2.88	1.76	1.34	1.1	0.897
Frequency (MHz) post-layout	233	125	350	200	540	200
Power (mW/MHz) post-layout	0.464	0.412	0.199	0.164	0.174	0.109

130G and 90G are with TSMC Sage-X libraries.
65GP is with TSMC Advantage library, Regular Vt.
Area and frequency at worst operating condition (0.9 * Vdd, 132 C)
Power at typical operating condition (1.0 * Vdd, 25 C)

Diamond 545CK Block Diagram



Instruction Set Architecture

The Diamond Standard Series implements the Xtensa® Instruction Set Architecture (ISA) a 32-bit RISC architecture featuring a compact instruction set optimized for embedded designs. The architecture has a 32-bit ALU, 32 or 64 general-purpose physical registers, 6 special purpose registers, and 80 base instructions. The Xtensa ISA employs 24-bit instructions with 16-bit narrow encodings for the most common instructions. These 16-and 24-bit instruction words are freely intermixed to achieve higher code density without compromising application performance. The Xtensa ISA thus optimizes the size of the program instructions by minimizing both the static number of instructions (the instructions that constitute the application program) and the average number of bits per instruction.

The use of 24- and 16-bit instruction words, the use of compound instructions, the richness of the comparison and bit-testing instructions, zero-overhead-loop instructions, register windowing, and the use of encoded immediate values all contribute to the Diamond processors' small code size. Thus, the 24-/16-bit Diamond processor ISA enables designers to achieve 25% to 50% lower code size compared to conventional 32-/16-bit ISA-based RISC cores. Reducing code size results in smaller memory sizes and lower power dissipation – key parameters in cost-sensitive, highly integrated SOC designs

The Xtensa ISA also provides powerful compare-and-branch instructions, zero-overhead loops, and bit manipulations including funnel shifts and field-extract operations.

Comprehensive Software Tool Support

A full-featured development environment – the Xtensa Xplorer™, Diamond Edition – provides a graphical user interface (GUI) to all code development tools. The compiler toolchain and instruction set simulator (ISS) are available through the GUI in addition to performance modeling tools. Based on the Eclipse framework, Xtensa Xplorer allows developers to quickly evaluate code on the pipeline-accurate ISS and interface to emulation and hardware development boards. Xtensa Xplorer serves as the cockpit for the entire development experience and integrates the compiler tool chain as well as the ISS and interfaces to hardware emulation/development boards.

Tensilica's XCC C/C++ compiler is an optimizing compiler that employs sophisticated multi-level optimizations to increase code execution performance and reduce code size. Also, XCC bundles multiple operations into VLIW instructions for the multi-issue Diamond processors (570T, 330HiFi, and the 545CK). Furthermore, XCC delivers enormous benefits to users of Tensilica's DSP engines through automated vectorization of C and C++ source code.

Also included in the Xtensa Xplorer environment are a software project manager, code profiling tools, a source code editor, a debugger, a performance-modeling tool, the Xenergy energy estimation tool, a cache performance explorer, and graphical visualization tools. Tensilica also provides both a C-based modeling environment called XTMP and SystemC models of the Diamond processors. See Tensilica's Software Developer's Toolkit product brief for more information.



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