



Diamond Standard 212GP Controller

A High-Performance General-Purpose RISC CPU

Product Brief

FEATURES

- High performance with minimal die area, low power
- 5-stage pipeline
- Dhrystone 2.1: 1.38 DMIPS/MHz
- 24/16-bit ISA with modeless switching
- Iterative 32x32 multiplier and 32-bit integer divider
- 16-bit DSP instructions
- 8Kbyte, 2-way instruction and data caches
- 2x32-wire GPIO ports for direct control and monitoring of peripherals
- Integrated interrupt controller with 22 interrupts and 6 priority levels
- Three integrated timers
- Single cycle XLMI interface for co-processors and devices
- On-chip debugging hardware
- Embedded trace support
- Comprehensive software development environment
- AHB-lite and AXI bridges

BENEFITS

- Flexible memory architecture adaptable to an extremely wide range of applications
- High arithmetic and DSP performance, reducing need for separate DSP
- High performance on general-purpose code
- No contention between instructions and data
- Fast and flexible interrupt handling
- Drop into existing AMBA™-based SOCs

Includes DSP Hardware Support

The Diamond Standard 212GP includes extra arithmetic and DSP hardware support, reducing the need to include a separate DSP in your system design.

A Flexible Mid-Range RISC Controller

The Diamond Standard 212GP CPU is a high-performance, fully synthesizable 32-bit RISC core. It is area and power efficient with a local memory architecture that provides outstanding flexibility and performance. Designers can take advantage of Tensilica's lockable cache and attach any size single-cycle instruction or data SRAM up to 128Kbytes.

Since the Diamond 212GP's target applications are controller related, interrupt options are extremely important. The Diamond 212GP includes a non-maskable interrupt for critical system events and six levels of interrupt priorities from a combination of external, software and timing interrupts. This eases the development of software interrupt handlers and external interrupt priority hardware design.

Arithmetic and DSP hardware support reduces the need to include a separate DSP in the system design. DSP support consists of a single-cycle 16x16 MAC unit adding four dedicated 32-bit registers and a 40-bit accumulator. Additionally, there is support for zero overhead looping, clamps (saturating arithmetic), max/min value, normalize, and sign extend. Arithmetic support is provided by a built-in 32x32 multiplier and 32-bit integer divider.

The Diamond 212GP features innovative I/O that allows data to be streamed in and out of the processor without going over the main data bus. The two 32-wire GPIO (general-purpose I/O) ports allow direct control and monitoring of peripherals.

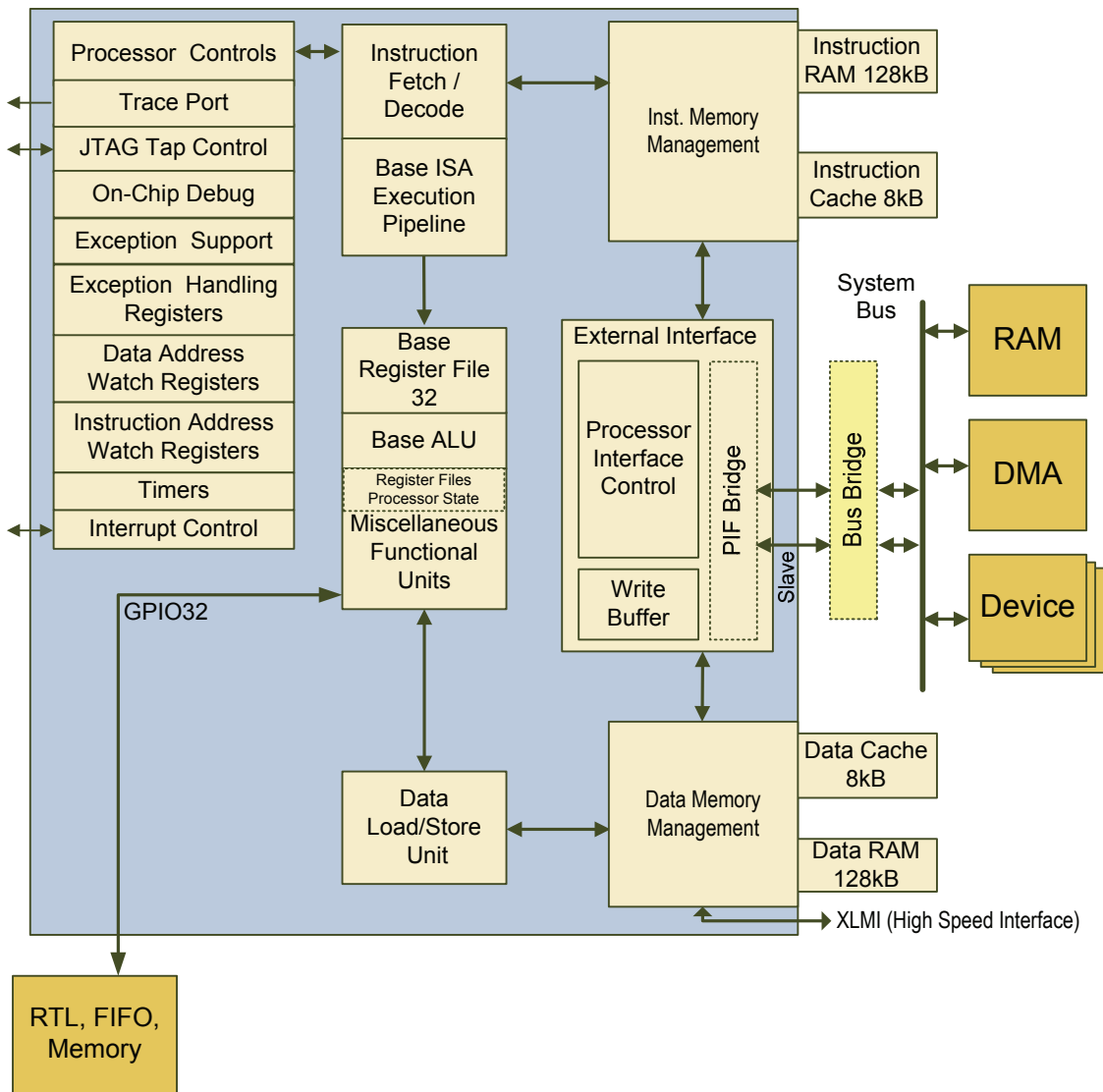
The performance of the Diamond 212GP is extremely high: 672 MHz in a 65gp process. It is capable of handling many control plane and DSP applications because of the built-in 32x32 multiplier and 32-bit integer divider.

Instruction Set Architecture

The Diamond Standard Series implements the Xtensa® Instruction Set Architecture (ISA) a 32-bit RISC architecture featuring a compact instruction set optimized for embedded designs.

The Xtensa ISA employs 24-bit instructions with 16-bit narrow encodings for the most common instructions. These 16-and 24-bit instruction words are freely intermixed to achieve higher code density without compromising application performance. The Xtensa ISA thus optimizes the size of the program instructions by minimizing both the static number of instructions





The Diamond Standard 212GP

Instruction Set Architecture (Cont.)

(the instructions that constitute the application program) and the average number of bits per instruction.

The use of 24- and 16-bit instruction words and compound instructions, the richness of the comparison and bit-testing instructions, zero-overhead-loop instructions, register windowing, and the use of encoded immediate values all contribute to the Diamond processors' small code size. The 24-/16-bit Diamond

processor ISA enables designers to achieve 25% to 50% lower code size compared to conventional 32-/16-bit ISA-based RISC cores.

Reducing code size results in smaller memory sizes and lower power dissipation – key parameters in cost-sensitive, highly integrated SOC designs.

The Xtensa ISA also provides powerful compare-and-branch instructions, zero-overhead loops, and bit manipulations including funnel shifts and field-extract operations.





Comprehensive Software Tool Support

A full-featured development environment – the Xtensa Xplorer™ – provides a graphical user interface (GUI) to all code development tools. The compiler toolchain and instruction set simulator (ISS) are available through the GUI in addition to performance modeling tools. Based on the Eclipse framework, Xtensa Xplorer allows developers to quickly evaluate code on the pipeline-accurate ISS and interface to emulation and hardware development boards. Xtensa Xplorer serves as the cockpit for the entire development .

Tensilica's XCC C/C++ compiler is an optimizing compiler that employs sophisticated multi-level optimizations to increase code

execution performance and reduce code size. Also included in the Xtensa Xplorer environment are a software project manager, code profiling tools, source code editor, debugger, performance-modeling tool, the Xenergy™ energy estimation tool, the cache performance explorer, and a number of graphical visualization tools. Tensilica also provides both a C-based modeling environment called XTMP, as well as SystemC models of the Diamond processors. For fast-functional simulation, Tensilica offers TurboXim for a 40-80x faster simulation than the ISS. See Tensilica's Software Developer's Toolkit product brief for more information.

Specifications

	65gp		65lp		45gs		40lp	
Flows:	High-Speed	Low-Power	High-Speed	Low-Power	High-Speed	Low-Power	High-Speed	Low-Power
Post-route cell area (mm²)	0.299	0.181	0.316	0.175	0.139	0.113	0.204	0.117
Speed (MHz) post Prime Time	672	58	416	57	835	58	536	57
Post-Route Power (mW/MHz)	0.078	0.046	0.103	0.041	0.048	0.027	0.067	0.039

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