



108Mini RISC Controller Core

PRODUCT BRIEF

(Revision B)

FEATURES:

- Ultra-low power, small area RISC controller
- Cache-less processor with memory protection unit
- 5-stage pipeline
- Dhrystone 2.1: 1.38 DMIPS/MHz
- 24/16-bit ISA with modeless switching
- 32x32 multiplier and 32-bit integer divider
- Separate instruction and data memory interfaces
- Dual local data RAMS
- 32-bit input/output GPIO pins for direct communication
- Integrated interrupt controller with 22 interrupts at 6 priority levels
- Three integrated timers
- On-chip debugging hardware
- Comprehensive software design environment
- AHB-lite and AXI bridges

BENEFITS:

- Lower total die area due to smaller core area and better code density
- Deterministic real-time operation through single cycle local instruction and data SRAMs
- Achieve high frequency: 400 MHz in 90G
- High arithmetic and DSP performance
- No memory contention between instructions and data
- Dual data RAMS allow ping-pong – read/write one, DMA into other
- Fast and flexible interrupt handling
- Drop into existing AMBA™-based SoCs

The Diamond Standard 108Mini CPU is a fully synthesizable 32-bit RISC CPU controller core. It is a small, cache-less RISC controller with tightly-coupled local instruction and data memories, a rich interrupt architecture, and high arithmetic and DSP performance. It enables SOC architects to integrate an efficient CPU in their designs, with the added benefit of extremely quick time-to-market. The Diamond 108Mini features class-leading low-power consumption for portable applications.

Although the Diamond 108Mini is smaller in die area than comparable 32-bit CPUs, its performance is extremely high: 420 MHz in a 90nm G process and achieving 1.34 Dhrystone MIPS/MHz. It also achieves high performance on DSP applications and engine and motor control applications because of the built-in 32x32 multiplier and 32-bit integer divider.

The Diamond 108Mini delivers fast and flexible interrupt handling with the availability of low interrupt latency and a rich interrupt architecture. The processor has deterministic behavior for applications with hard real-time constraints. 32 base registers are windowed 16 at a time, which enables much faster context switching due to reduced stack operations. Local single-cycle SRAM allows time critical code to be placed near the CPU. Dual local data SRAM enables processor access to one bank of RAM while an external DMA operation can operate on the other bank. Separate instruction and data memory interfaces lead to lower contention than unified interface architectures.

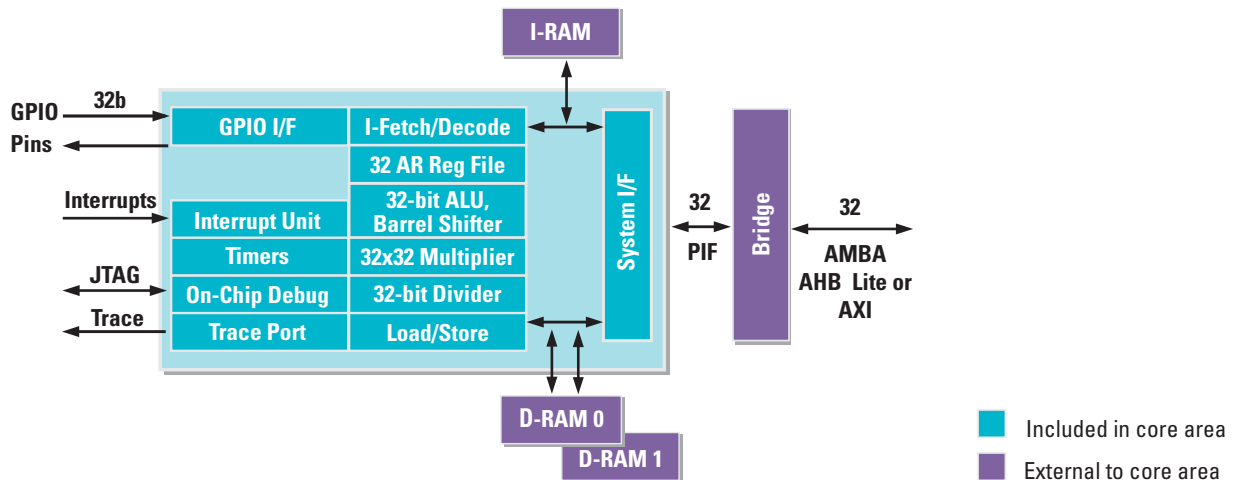
While small and low power, the Diamond 108Mini achieves the performance levels of much larger, complex CPUs.

Dhrystone: 1.34 DMIPS/MHz

Representative Performance/Area/Power	130G		90G		65GP	
	Speed Optimized	Area Optimized	Speed Optimized	Area Optimized	Speed Optimized	Area Optimized
Area (mm ²) post-synthesis	0.55	0.47	0.29	0.24	0.18	0.134
Cell area (mm ²) post-layout	0.72	0.53	0.36	0.26	0.247	0.143
Frequency (MHz) post-layout	250	125	400	200	660	300
Power (mW/MHz) post-layout	0.17	0.135	0.076	0.062	0.065	0.041

130G and 90G are with TSMC Sage-X libraries.
 65GP is with TSMC Advantage library, Regular Vt.
 Area and frequency at worst operating condition (0.9 * Vdd, 132 C)
 Power at typical operating condition (1.0 * Vdd, 25 C)

Diamond 108Mini Block Diagram



Instruction Set Architecture

The Diamond Standard Series implements the Xtensa® Instruction Set Architecture (ISA) a 32-bit RISC architecture featuring a compact instruction set optimized for embedded designs. The architecture has: a 32-bit ALU; 16, 32, or 64 general-purpose physical registers; six special purpose registers; and 80 base instructions. The Xtensa ISA employs 24-bit instructions with 16-bit narrow encodings for the most common instructions. These 16- and 24-bit instruction words are freely intermixed to achieve higher code density without compromising application performance. The Xtensa ISA thus optimizes the size of the program instructions by minimizing both the static number of instructions (the instructions that constitute the application program) and the average number of bits per instruction.

The use of 24- and 16-bit instruction words, the use of compound instructions, the richness of the comparison and bit-testing instructions, zero-overhead-loop instructions, register windowing, and the use of encoded immediate values all contribute to the Diamond processors' small code size. Thus, the 24-/16-bit Diamond processor ISA enables designers to achieve 25% to 50% lower code size compared to conventional 32-/16-bit ISA-based RISC cores. Reducing code size results in smaller memory sizes and lower power dissipation – key parameters in cost-sensitive, highly integrated SOC designs.

The Xtensa ISA also provides powerful compare-and-branch instructions, zero-overhead loops, and bit manipulations including funnel shifts and field-extract operations.

Comprehensive Software Tool Support

A full-featured development environment – the Xtensa Xplorer™, Diamond Edition – provides a graphical user interface (GUI) to all code development tools. The compiler toolchain and instruction set simulator (ISS) are available through the GUI in addition to performance modeling tools. Based on the Eclipse framework, Xtensa Xplorer allows developers to quickly evaluate code on the pipeline-accurate ISS and interface to emulation and hardware development boards. Xtensa Xplorer serves as the cockpit for the entire development experience and integrates the compiler tool chain as well as the ISS and interfaces to hardware emulation/development boards.

Tensilica's XCC C/C++ compiler is an optimizing compiler that employs sophisticated multi-level optimizations to increase code execution performance and reduce code size.

Also included in the Xtensa Xplorer environment are a software project manager, code profiling tools, a source code editor, a debugger, a performance-modeling tool, the Xenergy energy estimation tool, a cache performance explorer, and graphical visualization tools. Tensilica also provides both a C-based modeling environment called XTMP and SystemC models of the Diamond processors. For fast-functional simulation, Tensilica offers TurboXim, which offers 40-80x faster simulation than the ISS. See Tensilica's Software Developer's Toolkit product brief for more information.



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