



# DIAMOND

## STANDARD PROCESSORS

### FEATURES

- 32-bit RISC-style architecture with 5-stage pipeline
- 16/24-bit Instruction encoding (also 64-bit VLIW encoding on some cores)
- Compiler optimizes instruction length for high code density, modelessly switching between instruction types
- Fine and coarse-grained clock gating for ultra-low power
- AMBA AHB-lite and AXI bus interfaces
- Flexible direct Ports (GPIOs) and Queues (FIFOs) bypass the bus, speeding I/O on most models

### BENEFITS

- Extremely efficient base architecture is smaller, lower power, and has better code density than other comparable 32-bit RISCs
- Single architecture with extremely wide performance range covers most controller and DSP application tasks
- CPUs are upward compatible (106Micro -> 108Mini -> 212GP -> 232L -> 570T)
- Quick time-to-market through utilization of off-the-shelf synthesizable CPU or DSP IP
- Broad silicon supplier support for the Diamond series minimizes IP evaluation effort and risk
- Low power for portable applications

Tensilica's Diamond Standard Series processor family of synthesizable cores range from the industry's smallest 32-bit, ultra-low power, cache-less RISC controller to the industry's highest performance licensable DSP and most popular audio processor and an exciting video processor family. The Diamond Standard family covers the broadest range of performance of any embedded computing architecture.

The Diamond Standard processor family is based on Tensilica's highly efficient Xtensa® configurable and extensible processor architecture, proven in hundreds of SOC (system-on-chip) designs. Therefore, it's easy for designers to bridge to Tensilica's Xtensa processor product line if additional customization is required.

The Diamond Standard processors are supported by an optimized set of Diamond Standard software tools and a wide range of industry infrastructure partners, ranging from top-tier ASIC and foundry partners to companies that provide operating system support, co-verification, in-circuit emulation, EDA tools, and more.

#### Diamond Standard Series Lineup

##### Controllers

Diamond 106Micro	Smallest 32-bit, ultra-low power, cache-less RISC controller with local memories
Diamond 108Mini	Small cache-less RISC controller with local memories and right interrupt architecture
Diamond 212GP	Mid-range RISC controller with DSP instructions, I/D caches, TCMs

##### CPUs

Diamond 232L	Mid-range CPU with MMU for Linux, DSP instructions, I/D caches
Diamond 570T	Very high-performance CPU with 3-issue VLIW architecture

##### DSPs

Diamond 545CK	Very high-performance general-purpose DSP with 3-issue VLIW, 8-Way SIMD architecture
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##### Audio/Video Engines

Diamond 330HiFi	Low-power, 24-bit audio processor for all popular audio and speech codecs. Based on market-leading Xtensa HiFi2 audio engine
Diamond 388VDO	Low-power video engine supporting H.264 Main Profile decode, MPEG-4 decode, VC-1/WMV9 decode, MPEG-2 decode, and MPEG-4 Advanced Simple Profile encode



Check out our web site for the free 15-day Diamond software evaluation.

## AUDIO CORE

The Diamond 330HiFi core is optimized for 24-bit digital audio processing. See Tensilica's web site for a complete list of the popular audio codecs that have been ported to the Diamond 330HiFi core.

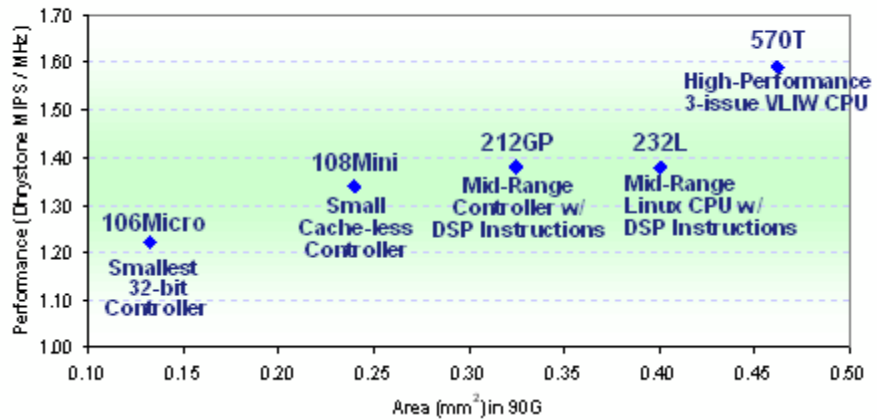
## VIDEO CORE

The Diamond Standard 388VDO Video Engine is optimized for multi-standard, multi-resolution video. Resolutions up to 720x480 (NTSC) and 720x576 (PAL) are supported, as are lower resolutions including QCIF, QVGA, CIF and VGA.

## DSP CORE

The Diamond Standard 545CK is the highest performance licensable DSP IP core, according to BDTI. The Diamond 545CK, which combines a base CPU controllers and a DSP containing eight parallel 16-bit single-cycle MAC units, allows system control and industry leading data processing throughput in a single core with a single compiler and single instruction stream. The Diamond 545CK can sustain eight simultaneous MAC operations on independent data pairs per cycle, utilizing the 160-bit vector registers.

### From cache-less controller to high-performance VLIW CPU



**Diamond Standard Processor Cores**  
The Largest Family of Upward Compatible Processors

Diamond Standard Controllers/CPU Selector Guide					
Characteristic	106Micro	108Mini	212GP	232L	570T
Max Frequency (90nm G)	400 MHz	400 MHz	400 MHz	350 MHz	400 MHz
Dhrystone MIPS/MHz	1.22	1.34	1.38	1.38	1.59
Area, post-synthesis (90nm G)	0.13 mm <sup>2</sup>	0.24 mm <sup>2</sup>	0.32 mm <sup>2</sup>	0.40 mm <sup>2</sup>	0.46 mm <sup>2</sup>
Area, post layout (routing efficiency) (90nm G)	0.145 mm <sup>2</sup> (85%)	0.26 mm <sup>2</sup> (85%)	0.36 mm <sup>2</sup> (85%)	0.44 mm <sup>2</sup> (85%)	0.52 mm <sup>2</sup> (65%)
Power, mW per MHz (90nm G, typical conditions)	0.044	0.062	0.089	0.096	0.124
# Pipeline Stages	5	5	5	5	5
Instruction Width	16/24 bit	16/24 bit	16/24 bit	16/24 bit	16/24/64 bit 3-issue
General Purpose I/O Ports	No	Yes	Yes	Yes	Yes
High-Throughput Data Queues (FIFOs)	No	No	No	No	Yes

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