

Seamless HW/SW Integration Environment

Xtensa and Diamond Standard Series Processor Support Packages



D A T A S H E E T

“Seamless is a key component of the tightly integrated hardware and software development tool suite we offer our customers. Prior to tape-out, customers can now make area, speed, power, and code density adjustments on a virtual platform, allowing design tradeoffs before silicon, avoiding unnecessary silicon re-spins.”

Chris Rowen – President and CEO, Tensilica, Inc.

Hardware/Software Integration for Configurable Processor Cores

Every embedded design requires hardware and software to work compatibly. Postponing verification of the design until the hardware is ready exposes design teams to the prospect of a lengthy validation process and increases the risk that a rebuild or re-spin of hardware will be required. Verifying a design before fabrication requires a productive environment for validating hardware and software together. As electronic designs become ever more complex, the need for effective hardware/software (HW/SW) integration for embedded systems design increases proportionally.

The Seamless® HW/SW integration environment from Mentor Graphics® creates a virtual prototype of a completed embedded system months before a physical prototype can be engineered. By executing embedded software on simulated hardware,

the Seamless environment allows you to fully verify the HW/SW interface and surrounding hardware, accelerate the debug of firmware, and analyze the performance of your chosen implementation — all before you commit to building the hardware.

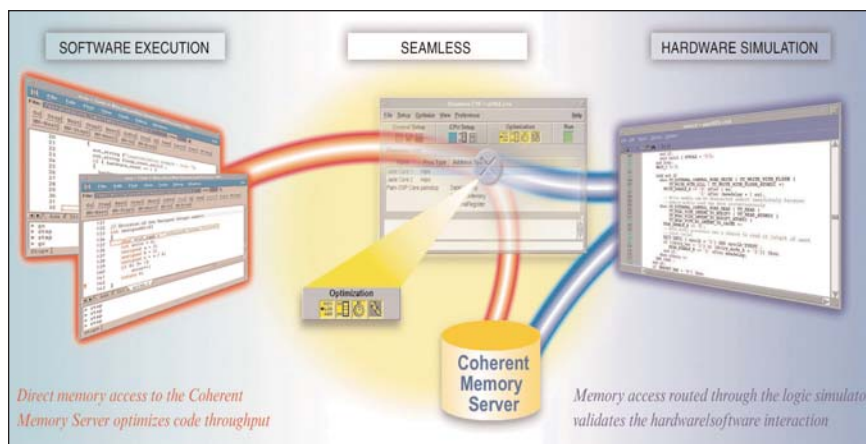
Mentor Graphics has partnered with Tensilica, Inc., a leader in the configurable processor marketplace, to create co-verification models for synthesizable Xtensa configurable cores and the Diamond Standard processors, which consists of six, off-the-shelf synthesizable cores ranging from area-efficient, low-power controllers to the industry’s highest performance DSP and popular audio processor. The Seamless HW/SW integration environment enables systems developers incorporating Xtensa and Diamond cores to validate HW/SW interfaces in a virtual prototype prior to fabrication of the design.

PSP product features:

- Processor Support Packages for the Extensa LX core and Diamond Standard 108Mini, 212GP, 232L, 570T, 330HiFi, and 545CK processor cores
- High-performance cores incorporate the instruction set simulator (ISS) and bus interface models (BIM) for all Xtensa and Diamond configurations
- Full visibility and control of hardware and software execution
- Enables efficient debug of hardware, firmware, and software early in the design process
- Dynamic optimizations provide performance four to five orders of magnitude above logic simulation without compromising debug
- Easy to use:
 - No software changes required
 - Drops into all popular hardware verification environments
- Charts key design performance characteristics
- Verified against vendor test suites

Seamless co-verification product benefits:

- Detects and isolates HW/SW interface errors months ahead of hardware prototype
- Reduces risk of schedule slip at system integration
- Eliminates HW prototype iterations
- Accelerates software debug, removing it from the critical path
- Identifies HW/SW performance bottlenecks



Seamless First to Support the Diamond Standard Series

Seamless is the first HW/SW integration tool to support Tensilica's Diamond Standard series, providing designers with unparalleled ability to debug hardware/software interactions while exercising production-level software on Seamless models of the Diamond Standard series processor cores. "We gave Seamless premier tool status because it provides our customers with the most effective methodology for debugging hardware/software interactions in our Diamond series of processor cores," said Steve Roddy, Tensilica's Vice President of Marketing. "By offering Seamless processor support packages upon introduction of the Diamond family, Mentor Graphics is enabling first-pass success for designers who choose to implement these advanced, cost-effective processor cores."

Bringing it All Together

The ever-increasing complexity of bridging hardware and system software places tremendous pressure on engineers charged with integrating these two components in a functional system. The ability to fully verify a design before committing to a physical prototype streamlines the design process for *both* the hardware and software teams. A virtual prototype provides the most productive environment for debugging software and

Processor Family	PSP*	Availability
Xtensa ¹	Xtensa LX	Released
Diamond Standard ²	108Mini	Released
	212GP	Released
	232L	Released
	570T	Released
	330HiFi	Released
	545CK	Released

* All PSPs are instruction accurate, available on Solaris and Linux, support by XRAY® and Xplorer debuggers. Linux support for PowerPC PSPs is based on customer demand.

1 - Supported logic simulators include NC-SIM and VCS.

2 - Supported logic simulators include NC-SIM and VCS.

correcting problems found in hardware or software before the hardware is fixed in implementation. By integrating existing HW/SW development flows, Seamless creates a common environment based on a single reference model, which enables simultaneous verification of HW/SW early in the design cycle. Providing the ability to verify, characterize, and debug complex embedded systems early means optimal designs on shorter schedules, with a greater chance at first-pass success.

Patented memory management and simulator interfaces — optimizations in Seamless — enable software-intensive tasks to be executed in orders of magnitude faster than in logic simulation.

Seamless combines the full hardware visibility of a logic simulator with a graphical source-level software debugger, allowing quick isolation of design errors. With Seamless, embedded software and hardware arrive at system integration completely verified and ready to go.

The Mentor/Tensilica combination enables greater verification efficiency for engineers who are trying to balance processor price and performance in order to deliver high-quality, low cost electronics to market on time. The Seamless HW/SW integration environment gives you the ability to make intelligent tradeoffs between detail and performance at different times during the design cycle.

Visit www.mentor.com/seamless for the latest product news.

© 2006 Mentor Graphics Corporation. All Rights Reserved.
Mentor Graphics, ModelSim, Seamless, and XRAY are registered trademarks of Mentor Graphics Corporation.
All other trademarks mentioned in this document are trademarks of their respective owners.



Tensilica, Inc.
Corporate Headquarters
3255-6 Scott Boulevard
Santa Clara
CA 95054-3013 USA
www.tensilica.com

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503.685.7000
Fax: 503.685.1204

Sales and Product Information
Phone: 800.547.3000

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408.436.1500
Fax: 408.436.1501

North American Support Center
Phone: 800.547.4303

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics (Taiwan)
Room 1001, 10F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886.2.87252000
Fax: 886.2.27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81.3.5488.3033
Fax: 81.3.5488.3004



04-06 MGC

1024770-w