

Tensilica's Diamond Standard Processor Cores

SOCcentral March 13, 2006 -- Well, just when you think you have the little scamps pinned down, the chaps and chapesses at Tensilica start bouncing up and down with some new ultra-cool "thing" with which to bedazzle and beguile us. The latest offering is a suite of processor cores that are collectively referred to as the "Diamond Standard" family (is this because they bring a little "sparkle" to one's designs?).

But before we leap into the fray with gusto and abandon to peruse and ponder these little rascallions, let's take a moment to remind ourselves as to just what it is the folks at Tensilica are famous for. Let's suppose you're going to create a system-on-chip (SOC) and you want to include one or more CPU and/or DSP cores. One option is to use standard pre-defined cores from a third party such as ARM or ARC. The problem is that these general-purpose cores may not give you the performance you need your our target application.

An alternative is to use the approach favored by Tensilica. In this case, you start off with an underlying 32-bit post-RISC engine called Xtensa that comprises around 25K logic gates. This little rascal has roughly the same performance as an ARM9 or a MIPS-32.

Now, let's assume that you have an application written in ANSI-standard C/C++ (say a video codec, for example). First, you would run Tensilica's XPRES Compiler, which will analyze the application and evaluate a humongous number of possible processor extensions based on techniques like single-instruction-multiple-data (SIMD) and vector operations, operator fusion, and parallel execution.

Following this evaluation, the XPRES Compiler will offer a selection of alternative configurations showing tradeoffs in terms of different architectures versus performance, gate counts, and power consumption. This lets you select the configuration that best meets the performance requirements of your application and the silicon area and power consumption requirements of your target environment. Next, you would run Tensilica's Processor Generator, which will output the RTL for your custom processor along with a custom compiler, assembler, and source-level debugger (Figure 1a). (It also generates, an instruction set simulator (ISS), which is omitted here for simplicity).

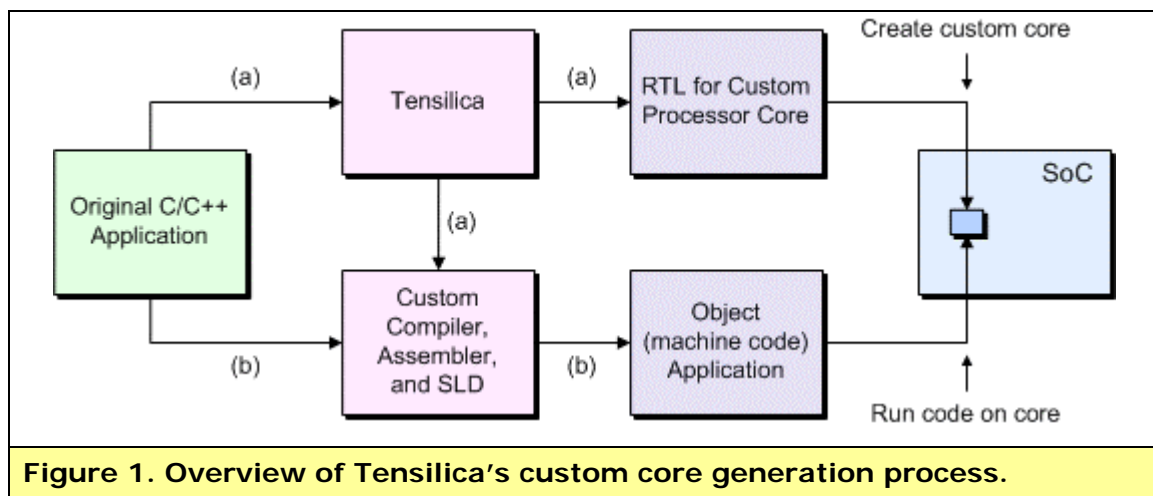


Figure 1. Overview of Tensilica's custom core generation process.

So now you have the register transfer level (RTL) representation for a custom core that you can implement on your SoC. Next, using your newly generated custom compiler, you would compile the original application into the executable (machine code) object file that will be run on your custom processor (Figure 1b). Or course, this compiler automatically recognizes operations that can be mapped onto the new instructions embodied in the custom processor.

The performance of these custom cores can be phenomenal. In many cases they achieve the same throughput we'd expect if you created a dedicated piece of hardware (with the added advantage that we can do the whole thing in less than a day). Also, these cores are extremely power-efficient, because the processor generator automatically inserts the code to implement extremely sophisticated clock-gating schemes (you might end up with 400 or more gated clock domains, which is way more than one would ever try to implement by hand).

It's important to note that the generated core isn't tied to the original application; this core will work just as well with any application of this general type. And, of course, you aren't limited to a single processor. You might decide to generate a special CPU-type core to perform some control-oriented applications along with one DSP-type core for video processing and another DSP-type core for audio processing. In fact, the folks at Tensilica say that the average user ends up with five or six heterogeneous cores on their SoCs (some implementations for networking applications have several hundred such cores).

Tensilica's New Diamond Standard Cores

So, since Tensilica folks provide us with the ability to generate custom cores, why have they decided to leap out with a suite of their own cores? One reason is that the Diamond Standard cores provide an easy entry point into Tensilica's technology. But the real bottom line is that some users simply do not wish to create their own core(s) from scratch; instead, they would prefer to leverage Tensilica's expert knowledge of key application domains.

So what exactly do we have here? Figure 2 provides a high-level positioning view of the six cores, which are named 108Mini, 212GP, 232L, 570T, 330HiFi, and 545CK (don't ask me about this naming convention, because [a] I don't have a clue where it came from and [b] I really don't want to know).

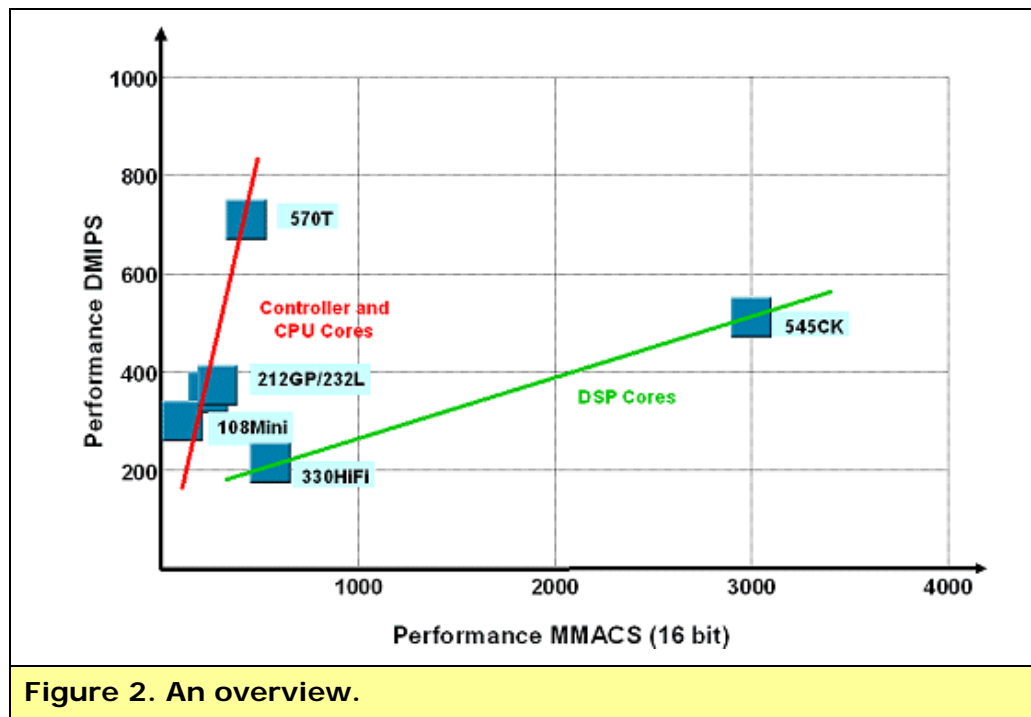


Figure 2. An overview.

The 108Mini Controller/CPU: This is the baby of the family. It's an ultra-low power, cache-less RISC controller featuring a rich interrupt architecture coupled with a minimal gate count for lowest silicon cost. In addition to a 32-bit system bus with an AMBA AHB-lite bridge (that lets the processor talk with standard peripherals from third-party suppliers), the 108Mini also features a very fast 32-bit input port and a 32-bit output port, greatly simplifying an SoC designer's life.

The 212GP Controller/CPU: For folks who want a bit more "ummmph," the 212GP is a flexible mid-range RISC controller with instruction and data caches and user-defined local memory sizes. Once again, in addition to a 32-bit system bus with an AMBA AHB-lite bridge, the 212GP features a very fast 32-bit input port and a 32-bit output port.

The 232L CPU: Next we have the 232L, which is very similar to the 212GP, except that it doesn't have the 32-bit input port and 32-bit output port. Instead, the 232L boasts a Memory-Management Unit (MMU), thereby making this a very flexible mid-range CPU that can fully support a Linux operating system.

The 570T CPU: When it comes to compute-intensive performance-critical applications, it's time to call out the big guns in the form of the 570T. Intended for those folks who really need serious processing power, this bad boy boasts a three-issue static superscalar CPU core and provides over twice the performance of an ARM11 (per MHz, based on EEMBC benchmarks).

The 330HiFi DSP: With regard to DSP-centric functions, the Diamond Standard family currently boasts two offerings. First we have the 330HiFi processor, which is targeted toward audio applications. Based on the market-leading Xtensa HiFi 2 audio engine, which is shipping in volume in cell phones, portable audio players, and multimedia/PVR chips, the 330HiFi boasts audio-centric features such as 24-bit MACs (required by high-quality audio processing algorithms) and support for all popular audio formats plus VoIP.

The 545CK DSP: Last, but certainly not least, when you have a monster DSP task to perform, the solution is the 545CK DSP core. Amongst many other features, the 545CK boasts a 64-bit Very Long Instruction Word (VLIW), a three-issue static superscalar CPU, eight 16-bit multipliers that can operate in single instruction multiple data (SIMD) mode, and a Viterbi accelerator for communications baseband applications. The result is the highest-performance licensable DSP that is faster than any other CPU or DSP core (BDTI Benchmarks from Berkeley Design Technology, Inc.). For example, the 545CK is 70% faster than its closest competitor, the CEVA-X1620.

Cool Beans

The Diamond Standard family of pre-configured cores is mega-cool for many reasons. First of all, it gives you access to off-the-shelf pre-configured cores that outclass anything else out there with regards to silicon real-estate, power consumption, or raw performance depending in the family member and what you're trying to achieve. Perhaps more important, this family shows just what can be achieved using Tensilica's configurable core technology. I for one am *VERY* impressed, and so it's a resounding "Cool Beans" from me!

Until next time, have a good one!



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